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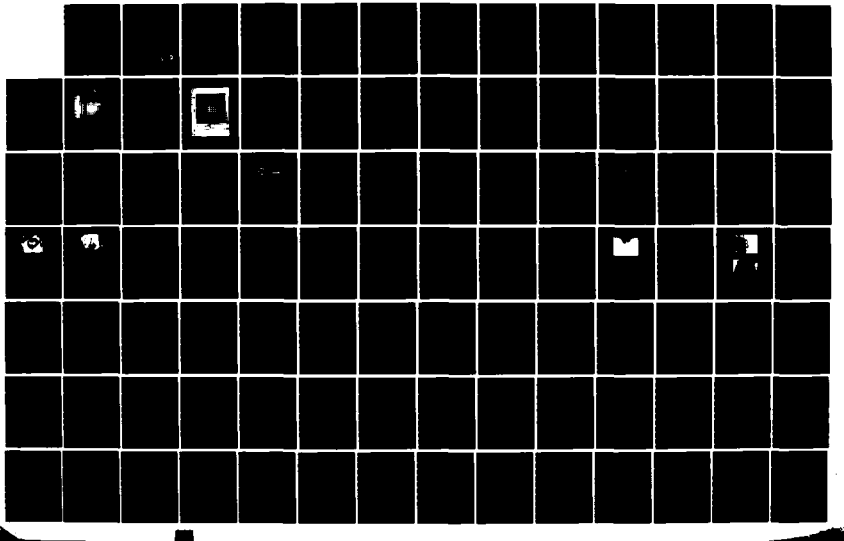

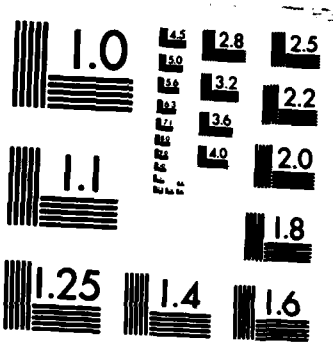

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ENCAPSULATION AND PACKAGING OF A SEMICONDUCTOR MULTIELECTRODE ARRAY FOR CORTICAL IMPLANTATION

THESIS

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AFIT/GCS/ENG/84D-30

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ENCAPSULATION AND PACKAGING OF A SEMICONDUCTOR MULTIELECTRODE ARRAY FOR CORTICAL IMPLANTATION

THESIS

Presented to the Faculty of the School of Engineering

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Requirements for the Degree of

Master of Science in Computer Engineering

Ricardo R. Turner, B.S.

Captain, USAF

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Preface

How the brain works is a mystery which remains unsolved. Although much is known of its function, much more is still unknown. A great deal of research is needed to understand how the brain works. If we can determine how it works, we can then build computers to duplicate this process. If a computer were to be able to see, comprehend what it has seen, then take the appropriate action, it could remove the human from hazardous situations. Placed in a missile, this computer could autonomously guide the weapon to a highly defended target, while the pilot remains safe outside of the defenses.

This thesis will not solve the mystery of the brain, or even answer any questions about it. However, it does provide a tool which can be used to conduct further research. By packaging an encapsulated brain chip, as I have described in this thesis, it will be practical to accomplish long-term monitoring of the brain signals produced by the neurons comprising the brain.

I would like to thank Dr. Roger Colvin and Dr. Matthew Kabrisky for the encouragement, motivation and technical support they provided me throughout my work. Since I am not an Electrical Engineer, their guidance and answers were as greatly appreciated as they were needed. I especially appreciate the many hours Dr. Colvin put in to help me learn and modify the integrated circuit processing equipment I had to use.

I would also like to express my gratitude to Mr. Don Smith, the AFIT processing laboratory technician, and Mr. Alva Karl from the Aerospace Medical Research Laboratory. Mr. Smith provided help daily

in keeping the equipment running. Mr. Karl was instrumental in helping me design the implantable package and the suggested surgical process.

Finally, I would like to thank my wife, Kaoru, and daughter, Charlotte, for supporting me throughout my long hours of work.

Ricardo R. Turner

Table of Contents

List of Figures

List of Tables

Abstract

A 16 X 16 multielectrode semiconductor array, known as the AFIT brain chip, must be encapsulated prior to implantation into the cerebral cortex of a rhesus monkey. The encapsulant, which must protect the chip from the saline-like solution of the cerebro-spinal fluid, was a polyimide: Dupont PI 2555. The polyimide was spun onto the chip, and the electrode openings etched, using negative photolithography and wet chemical etching. An eight-micron thick layer of polyimide was obtained by repeating this process several times. Although actual implantation was not performed, an implantable package was designed and fabricated which will allow for chronic use with only one surgical operation. A surgical technique for implanting the package is suggested. The fabricated package was not fully functional, however, because an epoxy used to protect bond wires from the stress of the polyimide could not withstand the high temperature cure. The functioning part of the chip was tested in vitro and worked continuously for three weeks. There was no damage to the polyimide encapsulant, but some of the aluminum electrodes showed signs of deterioration.

ENCAPSULATION AND PACKAGING OF A SEMICONDUCTOR MULTIELECTRODE ARRAY FOR CORTICAL IMPLANTATION

I. Introduction

Background

For many years, man has tried to decipher the structure of the brain, and how it works. Of particular interest is how the brain can transform data received from the eyes into a picture of the environment. Scientists have worked at getting computers to "recognize" objects seen through some type of optical sensor. This area of study, pattern recognition, has obvious uses in the military for "smart" weapons which can visually seek out targets and destroy them. However, getting a computer to understand what it sees is far from trivial. Dr. Kabrisky has theorized that a "blueprint" of the brain may aid in building computers which can duplicate some of the brain's functions (1:5).

A number of ideas have been put forth on how the brain functions. Lorente de No (1949), Mountcastle (1957), Hubel and Weisel (1962), and Kabrisky (1966) developed models which suggest bundles of neurons working as a functional element comprise the basic computing elements of the cerebral cortex. These basic computing elements (b.c.e.'s) measure about 50 to 100 microns in diameter in the human visual cortex (the portion of the brain concerned with vision) (1:40). Attempts to measure the output of adjacent b.c.e.'s have not succeeded due to the size of the b.c.e.'s and the size (and number) of the probes (2:5). The need existed to make the electrodes smaller and more closely spaced: to get as close to the actual size and density of the b.c.e.'s themselves.

This has led to the development of a multielectrode semiconductor which can be implanted onto the cortex to record actual measurements of the b.c.e. signals.

A number of thesis efforts, at the Air Force Institute of Technology (AFIT), have delved into the problem of directly measuring the brain's signals. The first effort, in 1979, was by Joseph Tatman. He proposed and designed a 100 X 100 multielectrode semiconductor array for the purpose of recording data from the cerebral cortex. This was simply a design for establishing the feasibility of this novel circuit. Tatman then fabricated a simpler 4 X 4 multielectrode array prototype based on this design. Unfortunately, the prototype circuit did not function (3:10-11). However, the ideas, results, and fabrication process which Tatman developed set the stage for further research.

Gary Fitzgerald continued this research the following year in his 1980 thesis. Fitzgerald successfully fabricated a 4 X 4 multielectrode array based on Tatman's prototype. Although the circuit functioned properly in a normal environment, it failed after 30 seconds in a saline bath test (4:108). This saline bath simulates the cerebrospinal fluid (CSF) environment found in the brain (4:9). The normal silicon dioxide (SiO_2) coating protecting the chip was not adequate to protect it from the CSF (4:109). The results of this thesis brought eventual success closer.

Solving the chip protection problem became the thesis effort of George German in 1981. Using Fitzgerald's AFIT brain chip array (as the 4 X 4 multielectrode had come to be known), German researched and evaluated different combinations of protective materials, and various methods of applying them to the chip. Based on his results, German

recommended two possibilities for further study as encapsulants (protective coatings): polyimide and phosphosilicate glass (PSG) (2:59).

With the chip fabricated and the possible encapsulant selected, Russell Hensley and David Denton continued the research to actual implantation in their 1982 joint thesis effort. They chose polyimide for encapsulating the chip based on German's results, its ease of processing, and its availability on Wright-Patterson AFB (5:9). Tests of the encapsulated chip in the simulated CSF environment (saline bath) proved successful (5:70), and the chip was surgically implanted into the visual cortex area of a laboratory beagle's brain. The chip recorded an enormous volume of electroencephalographic and visual evoked response information during the nineteen days it was in the dog's brain (5:88-89). When surgically removed from the brain, the chip showed some damage, caused either by the removal process or leakage of water into the chip (5:92). The exact cause was not determined due to the lack of time to analyze the chip. However, the chip functioned correctly and recorded valid data for over two weeks. The data it produced confirmed the validity of some major aspects of the theorized basic computing element structure of the cortex (5:93).

To continue research in the use of semiconductor cortical implants, Robert Ballentine, a student in the Graduate Electrical Engineering program at AFIT, designed and tested a new semiconductor array (Appendix E). This 16 X 16 multielectrode semiconductor array, shown in Figure 1, has sixteen times as many electrodes as the Hensley and Denton 4 X 4 array, yet is only one-fourth its size. Additionally, the new array utilized NMOS technology in contrast to all previous arrays which were JFETs.

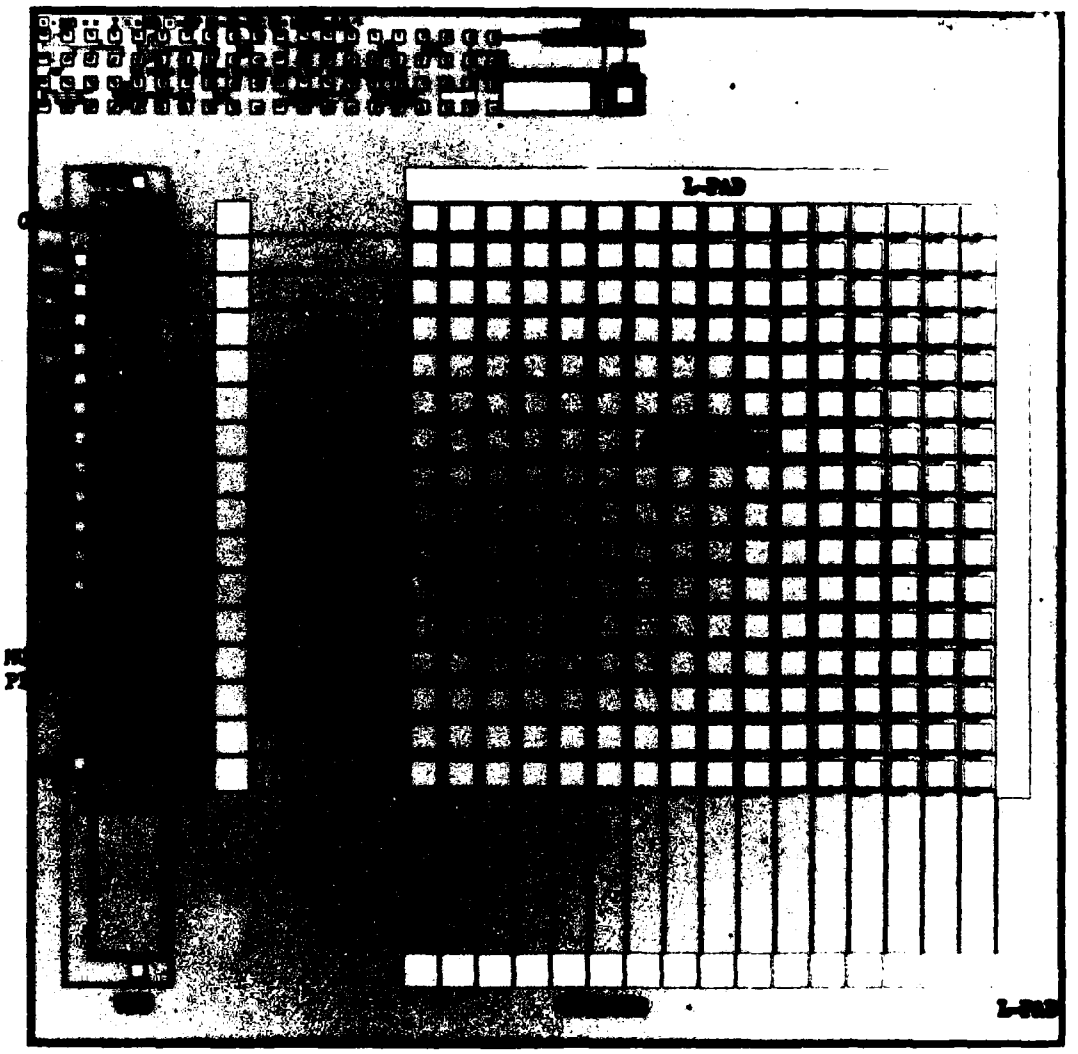

Figure 1. Brain Chip Array with Count Selectable Multiplexer

Besides the greater number of electrodes, the new array contains control circuitry to allow output of the 256 electrodes on only sixteen wires. This is done through use of a 4-bit counter and a 4 X 16 multiplexer. The counter and multiplexer function together to select one of

sixteen rows of the array. The selected row then sends the signals on its electrodes to the sixteen output pads to a recording device. Normally, the counter will select each row in sequence (one through sixteen), allowing all 256 electrodes to be monitored. However, using the count select inputs (CS0 - CS2), four, eight, or all sixteen rows can be monitored. Therefore, only 16 wires are needed to output the data from all 256 electrodes.

Additional features of this chip include enhancements for future use of two chips in synchronization. This is accomplished through the synch in (SYI) and synch out (SYO) pads. The synch in signal (from an external source) initiates the count sequence. The synch out signal is sent to SYI of the second chip when the counter finishes its sequence. The decoder determines when the count sequence finishes. Another feature involves the four tri-state pads (TS0 - TS3) which are controlled by CON. These pads allow monitoring of the output of the counter, or input of a simulated count (for test purposes). Full details of the chip's design can be found in Appendix E. Details of its testing are included in Appendix F.

Ballentine also designed a second 16 X 16 array, seen in Figure 2, which is similar to his original 16 X 16 array, but includes an additional multiplexer and counter to select the output columns, sequentially. This version requires only one wire to output the data, instead of sixteen. However, it did not function correctly in its initial production version, as can be seen in Appendix F.

One final thesis effort, not directly related to the brain chip efforts, was accomplished by Jayne La Voie in 1985. La Voie studied the use of polyimide as an integrated circuit insulation material, for

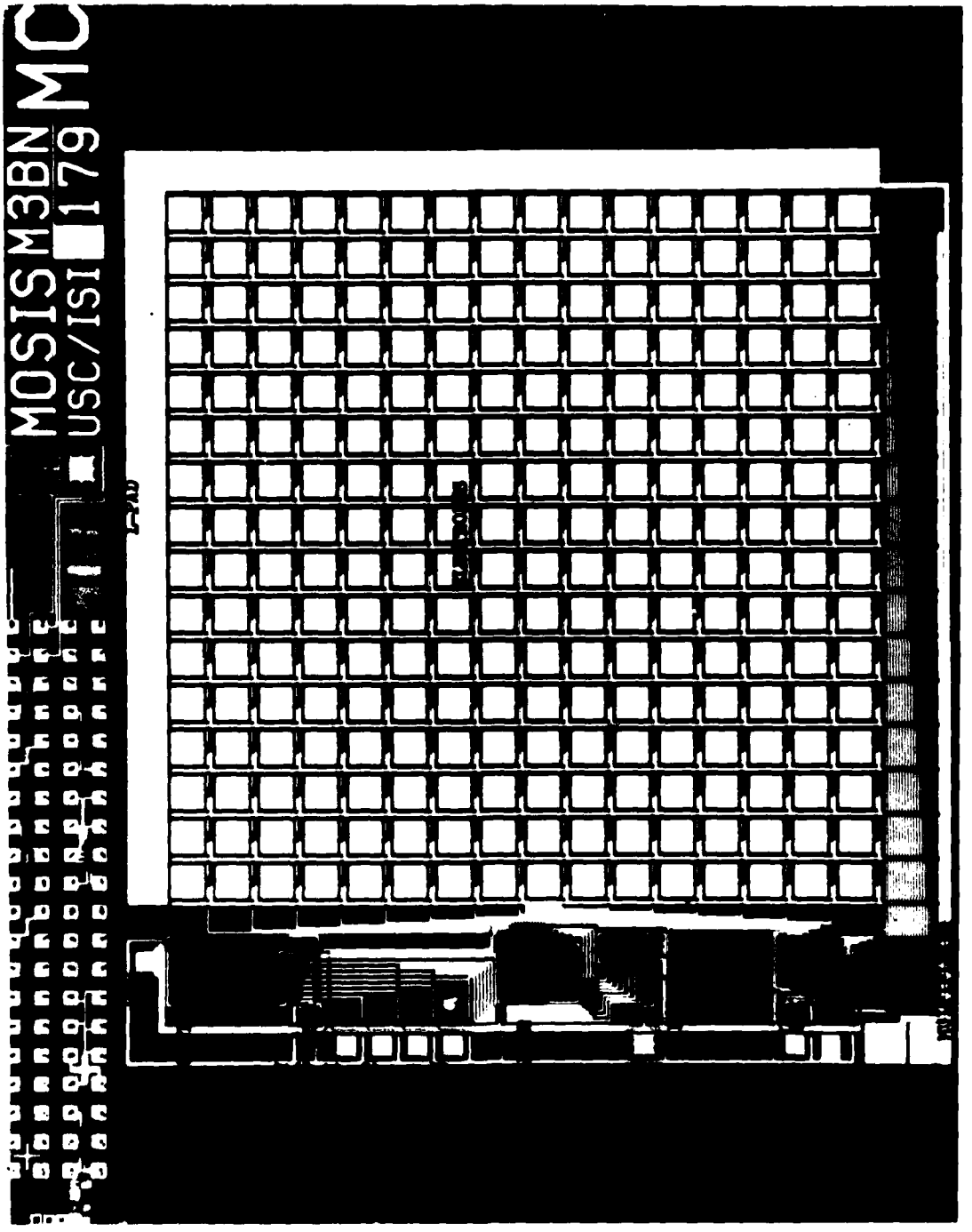

Figure 2. Brain Chip Array with Count Selectable Multiplexer and Multiplexed Outputs

the Avionics Laboratory at Wright-Patterson AFB. The procedures La Voie used to passivate, mask, and etch the polyimide have further refined the encapsulation process used by Hensley and Denton. La Voie recommended a specific etching technique, R-F plasma etching, for best results. He also recommended applying a thick layer of polyimide to decrease the pinhole defects (6:77).

Statement of Problem

Since a smaller brain chip has been fabricated, a new procedure must be developed to allow it to be implanted in a mammalian brain. This new procedure must minimize the surgery (and its associated trauma) while maximizing the longevity and reuseability of both the mammalian subject and the chip.

The problem, then, is to fabricate an implantable multielectrode semiconductor array which will survive the harsh environment within a mammalian brain for an extended period of time. The package for this chip will require a surgical operation for initial insertion only, and will allow nonsurgical removal and reinsertion.

The success of the Hensley and Denton brain chip implantation clearly demonstrated the feasibility of a using polyimide as an encapsulant for oranial implants. The 4 X 4 multielectrode functioned successfully for nearly three weeks in the corrosive cerebrospinal fluid of the dog's brain. However, their encapsulation involved a relatively large semiconductor.

The new brain chip, Ballentine's 16 X 16 multielectrode semiconductor array, has sixteen times as many electrodes as the 4 X 4 array. This increased number of electrodes fits into a smaller area than the

larger array, complicating the problem of lead attachment.

An additional problem which carries over from the previous implant is the surgery involved. Implantation of the chip into the dog's brain required 3-1/2 hours of major surgery (5:88). Although this surgery was successful, it can be a traumatic experience for the subject, especially if it must be performed for both insertion and removal. A non-surgical method allowing chronic implantation of the same subject must be developed.

Scope

The emphasis of this thesis will be to encapsulate and package a new multielectrode array device for chronic implantation, which will be impervious to cerebrospinal fluid (CSF) for an extended period of time (up to three weeks). This new device will be the 16 X 16 multielectrode array designed and tested by Ballentine. The package must be capable of being inserted into a grommet or cylinder which has been surgically inserted into the skull of the laboratory subject. This will allow the insertion and removal of the device without further surgery.

The new 16 X 16 array uses aluminum electrodes instead of the silver electrodes used by the previous arrays. Since it is not known how the exposed aluminum will function in the CSF environment, silver will be evaporated onto the electrodes of some of the chips to be encapsulated.

This effort will not explore untested encapsulating materials or processes, unless the existing materials and processes result in substandard, non-implantable devices. In addition, actual implantation will not be attempted as a part of this work. This will be

accomplished at a later time. A suggested procedure for implantation will, however, be discussed.

Assumptions

This thesis effort assumes that polyimide is an adequate encapsulant material. Although Hensley and Denton suggested water may have permeated the polyimide material, it will still be used since polyimide is available and has worked in the past. The passivation schedule which La Voie developed in his thesis is assumed valid. If this passivation schedule does not allow operation of the chip in a saline bath environment for the required minimum of nineteen days, other schedules will be attempted. Finally, it is assumed that the brain chips provided are functional, as their functionality will not be tested in this thesis.

Summary of Current Knowledge

Currently, this project is unique to AFIT. Much of the current knowledge in this area is in the theses cited in the background material. Although others have used implantable devices in vivo, there is little documentation of use of such devices in the brain. The choice of polyimide as the protective coating for the brain chip was based in part on German's research into a passivating material. This choice was made by Hensley and Denton due to its availability at AFIT (5:9). However, this does not imply that polyimide is the best material for protection from the CSF.

Polyimide is a high-temperature resistant, high strength superpolymer which exhibits a strong resistance to corrosive environments (7:727). Its primary advantage, as pertains to this thesis, is its

electrical properties. Polyimide is an excellent insulating material due to its low dielectric constant, low dissipation factor, and high volume resistivity. Typical values for the electrical properties of polyimides, as compared to similar insulating materials, appear in Table I. As seen in the table, polyimide, although not the best insulator, exhibits very good electrical properties. Due to these properties, polyimide is now used as an insulator between metal layers during integrated circuit fabrication (8:618).

TABLE I

Electrical Properties of Selected Polymers and Glasses (9:33)

Material	Dielectric Constant (at 60 Hz, unless otherwise stated)	Dielectric Strength (V/mil, 1/8" thick, unless otherwise stated	Dissipation Factor (at 60 Hz, unless otherwise stated)
ELASTOMERS*			
1. Polyurethane	6-8	850-1,000	0.276
2. Silicone Rubber	3.0-3.5 (at 1 kHz)	100-655	0.001-0.010 (at 1 kHz)
THERMOSETS*			
3. Epoxy (mineral filled)	3.5-5.0	300-400	0.010
4. Epoxy (glass filled)	3.5-5.0	300-400	0.010
5. Phenolic (glass filled)	7.1	140-400	0.050
6. Polyester (glass filled)	5.3-7.3	345-420	0.011-0.041
THERMOPLASTICS**			
7. Acrylic	3.3-3.9	400	0.04-0.05
8. Cellulose Acetate	3.2-7.5	290-600	0.01-0.10
9. Chlorotrifluoroethylene	2.65	450	0.015
10. Fluorinated ethylene propylene (FEP)	2.1	500	0.0002
11. Polytetrafluoroethane (PTFE)	2.1	400	<0.0001
12. Nylon 6	6.1	300-400	0.4-0.6
13. Nylon 6/6	3.6-4.0	300-400	0.014
14. Polyethylene (medium density)	2.3	450-1,000	0.0001-0.0005
15. Polyimide	3.5	400	0.002-0.003
16. Polypropylene	2.1-2.7	450-650	0.0007-0.005
17. Polystyrene	2.5-2.65	500-700	0.0001-0.0005
18. Polyvinyl Chloride (flexible)	5-9	300-1,000	0.06-0.15
19. Polyvinyl Chloride (rigid)	3.4	425-1,040	0.01-0.02
GLASSES**			
20. Borosilicate (#7740)	4.8	4,800 (kV/cm, 0.10 mm)	
21. Soda Lead	8.2	3,100 (kV/cm, 0.10 mm)	
22. Soda Lime	7.0	45 (kV/cm, 0.10 mm)	

The cerebrospinal fluid, a saline-like environment, contains a large amount of sodium ions. Sodium ions are one of the most damaging contaminants of integrated circuits: very small concentrations (a few parts per million) cancause catastrophic failure of a circuit (10:546). The silicon dioxide layer which initially protects the chip can retard penetration of moisture, but not of the sodium ions (10:548). The polyimide encapsulation, then, should adequately protect the integrated circuit from the harsh CSF environment. However, this protection may only be temporary. The temporary protection results from an important disadvantage: the water permeability of polyimides.

Polyimides, like most polymers, "possess a finite permeability to moisture" and water vapor (9:29). As moisture permeates throughout polyimide, it begins to raise the dielectric constant and dissipation factor of the polyimide (9:32). Therefore, a polyimide-encapsulated chip, left in the CSF for an extended period of time, will slowly lose its strong electrical properties, possibly allowing sodium ions to penetrate to the chip's surface. This time period, however, should be sufficient for the length of time the brain chip is to remain in the brain.

Besides moisture penetration, another problem which occurs with polyimides is their high rate of shrinkage. This shrinkage is great enough to pull bonds from their bonding pads (11:6). Despite these problems, polyimide does protect against sodium ions in the cerebrospinal fluid, for at least nineteen days, as proven by Hensley and Denton.

Approach

This problem will be solved using an approach which divides the

problem into six separate milestones.

1) Preliminary tests will be run to insure the electrodes can record data in a saline bath environment. A packaged chip (in a 64-pin package) will be coated around its perimeter, by hand, with polyimide. This package will be tested for proper operation in a normal environment, to insure proper functioning of the clock, counter, decoder, and multiplexer. The chip will then be tested in a saline environment with a signal applied to the electrodes. Since the package is encapsulated by hand, preliminary testing checks proper functioning of the chip, not the capability of the polyimide to protect.

2) An entire chip will then be encapsulated with polyimide following a passivation schedule similar to that used by Denton and La Voie. Using a mask, the aluminum electrodes and bonding pads will be exposed by etching through the polyimide. For maximum protection, the passivation schedule will be repeated five times forming a relatively thick layer of polyimide.

3) In parallel with encapsulating the chip, a package for inserting the chip into the brain will be designed. The AFIT Machine Shop will fabricate the design.

4) After encapsulation, the chip will be tested in a saline environment. This will determine the success of the encapsulation procedure.

5) At least four chips will be produced with silver electrodes, instead of aluminum electrodes. The silver will be evaporated onto the aluminum pads of the brain chip. These chips will then undergo the encapsulation process.

6) After encapsulation, both the silver and aluminum electrode

brain chips will be bonded to the packages fabricated by the Machine Shop. Long-term testing of both types of chips in a saline bath environment will then take place.

Sequence of Presentation

The sequence in which the material will be presented in this thesis differs slightly from the sequence of steps in the Approach. Chapter II discusses the design of the complete implantable package. This includes the requirements of the brain chip encapsulation and package design, the design of the package, and integration of the chip and package. A suggested procedure for implantation and insertion of the package is also included.

Chapter III discusses the actual encapsulation process for the chip. Starting with practice wafers, this chapter reveals how the final single-chip encapsulation process evolved. The addition of silver onto the electrodes of the chip is also included.

The results of saline environment tests on the brain chip are presented in Chapter IV. Tests are run on both an unencapsulated and encapsulated chip in a 64-pin package, and an encapsulated chip in the implantable package.

The problems encountered throughout this effort, especially in the encapsulation process using single chips are summed up in Chapter V.

Chapter VI discusses the conclusions reached about the encapsulation process and the completed package. Recommendations for follow-on research and package designs are also included.

II. Design of an Implantable Package

Designing an implantable package first requires setting down the rules, or requirements for the package. This can be broken into two areas: requirements for the brain chip and requirements for the package. Based on the requirements, the design of the package can be developed. The brain chip has already been fabricated, so only the actual proccessing will be discussed. This is done in Chapter III. The package which will hold the brain chip was not fabricated prior to this thesis, and its design and fabrication are discussed here. After the package is developed, it can be integrated with the brain chip into an implantable package. Although the actual implantation of the package is not covered, a recommended procedure for implantation is.

Requirements for the Array

As mentioned earlier, the brain chip array was designed by Ballentine. His design was to be an improvement over the 4 X 4 JFET array used by Hensley and Denton. This JFET array suffered from some flaws which became the basis for some of the requirements of the new brain chip array. Additionally, further refinement of an established procedure has led to new requirements.

The most important problem with the 4 X 4 array was its size. The chip measured one centimeter by one centimeter. Due to the curvature of the skull, and hence the brain, it becomes difficult to contact the complete surface of the chip with the brain. There is also a risk of local compression of brain tissue. Hensley and Denton stated that the 4 X 4 array was "somewhat large" for the laboratory beagle's skull

(5:90). The next research mammal to be used is the rhesus monkey, whose skull is only somewhat larger than that of a beagle. Therefore, a smaller brain chip is required to continue the research.

An inconvenience with the JFET array is its requirements for positive and negative voltages. Hensley and Denton powered their array from batteries supplying +6 volts and -6 volts, which is not TTL compatible (5:57). This requires use of negative logic. Also use of the JFETs requires "pinch-off" voltages for the transistors (which varied considerably from JFET to JFET) and a tedious "tuning" of the array to compensate for the differing DC offsets introduced by individual JFETs (5:45-49). To solve these problems, the new array should be fabricated from NMOS technology. This technology is directly TTL compatible, requiring only a +5 volt power source, and positive logic (12:157-158). Through MOSIS and DARPA, NMOS integrated circuits can be fabricated at no cost to AFIT.

The basic computational elements (b.c.e.'s) in the brain are approximately 50 to 100 microns in diameter in the human visual cortex (1:41), and as much as 500 microns in mammals such as cats (15:155). To allow observation of an individual b.c.e., the electrodes in the array must be of similar size. Therefore, the electrodes on the new array are required to be less than 500 microns wide, and should be as close to the 50 to 100 microns dimension as possible.

To allow simultaneous observation of more b.c.e.'s, the number of electrodes on the NMOS chip was increased from 16 to 256. However, an increase in the number of relatively large electrodes was accomplished in less space than that used by the 4 X 4 array chip due to the smaller size of the bonding pads.

An increase in the number of electrodes results in an increase in the number of outputs to the external world. This undoubtedly means an increase in the number of wires externally attached to the surface of the chip. However, the more wires attached, the larger the final package, and the greater the vulnerability to mechanical failure (due to breakage of wires). Therefore, control circuitry must be included on chip to minimize the number of wires which must be attached to the chip.

As with any VLSI circuit today, the new brain chip must be testable, to allow verification of correct functioning, prior to implantation. This requires test pads be added to allow monitoring of the control circuitry on the chip.

Finally, to allow long term use of the chip, it must be protected from the corrosive cerebrospinal fluid (CSF). This requires an encapsulant which resists penetration not only of moisture, but also of the numerous ions found in the CSF (see 14:533 for a list of these ions). Especially important is protection from the sodium ions, one of the most damaging contaminants to integrated circuits (10:546). However, an additional requirement here is that the chip and its protective layer be inert to brain tissue and the CSF. If it is not inert, the possibility of infection, or worse, permanent damage to the mammal, exists.

Most of the requirements, summarized in Table II, have already been met with the brain chip array designed by Ballentine, and modified by Dr. Roger Colvin. This array, seen in Figure 1, is smaller than the 4 X 4 JFET array. It measures 0.71 centimeters as compared to the 1.0 centimeters of the 4 X 4. Using NMOS technology, the number of electrodes was increased by a factor of 16 to 256, with each electrode measuring

Table II

Requirements for the Brain Chip Array

REQUIREMENT	REASON
Smaller chip size	Better contact with brain
NMOS technology	TTL compatibility; positive voltages
Small electrodes	Observe individual b.c.e.'s
More electrodes	Observe maximum number of b.c.e.'s simultaneously
Minimum number of wires	Smaller package; minimize mechanical failure
Test pads	Verify functionality of the chip
Protection from CSF	Long-term use of chip
Chip and protective layer inert to brain/CSF	Reduce chance of infection or damage to mammal

180 microns by 180 microns. The JFET electrodes of the 4 X 4 array measured 180 microns by 120 microns. The 250 micron center to center spacing was maintained for both versions. This puts the electrode size well below the theoretical size of the cat's b.c.e.'s (500 microns), although still larger than a human's.

By multiplexing the sixteen rows, the number of wires required to observe the 256 electrodes was minimized. Therefore, only sixteen wires are required to output signals to the external world. Finally, the chip is very testable, with special pads allowing monitoring of the circuit's clock pulses, counter, and multiplexer. This chip has been fully tested by Michael McConkey (Appendix F) and is fully operational. Further details on this chip may be found in Appendix E.

A modified version of this chip (Figure 2) was also designed by Ballentine. This modified version further reduced the number of wires required to observe the electrodes to only one wire. This was accomplished by adding a second multiplexer to multiplex the sixteen outputs. In doing this, some testability was lost. However, this chip, also tested by McConkey (Appendix F) does not function correctly. No attempt to correct this chip was made in this thesis.

The only remaining requirements for the brain chip array, then, are protection of the array from the CSF and protection of the CSF and brain from the chip/protective layer. Accomplishment of these requirements comprise Chapter III.

Requirements for the Package

The brain chip must be packaged in some manner to allow implantation into the skull. Hensley and Denton used the actual chip itself, glued to a silicon square of equal dimensions, as the package. The chip and wires were coated with epoxy (for strength) and polyimide (for protection) (5:26). The resulting package was fragile and had to be surgically implanted and surgically removed. The requirements for the package in this thesis are based upon many of the recommendations Hensley and Denton discussed for continued research.

The first requirement is that the package be reuseable, allowing chronic implantation and removal. This allows maximum use of the chip and the package. In addition, should a chip malfunction for any reason, it can be replaced.

With chronic insertion and removal comes the danger of trauma to the mammal subject which can incapacitate or kill. Therefore, the

package must be capable of insertion and removal with the least amount of trauma. Cranial surgery, then, must be minimized.

The next mammal to be used, a rhesus monkey, has a small skull. This requires that the package be small, to insure the chip will lie flat and completely against the brain despite the skull's (and thus the brain's) curvature.

Once implanted in the skull, the package must not exert any mechanical force which may damage the brain. Twisting the chip against brain tissue may rip and scar the tissue. On the other hand, exerting direct pressure on the brain (in an attempt to force it flat against the brain) can cause edema or necrosis (5:81). If the brain is damaged, the experiment will probably yield erroneous and misleading data.

As with the brain chip, the materials used in the package must be inert. There should be no reaction between the package and the brain tissue or CSF.

Along with being inert, the package must provide protection from penetration of infectious agents into the skull. The laboratory beagle used by Hensley and Denton showed signs of wound infection after seventeen days. The most probable cause was that infection traveled up the tubing protecting the wires. Therefore, the package must be able to seal out infection.

Finally, the package must be immovable when in place, and mechanically stable. Unlike a dog, a rhesus monkey has fingers with which to securely grasp something protruding from its head. In the cage, the monkey may knock the package against the bars. The package must be designed to prevent the monkey from damaging it, or injuring itself.

The requirements for the package are summed up in Table III. These

Table III

Requirements for the Brain Chip Package

REQUIREMENT	REASON
Chronically implantable	Maximum use of the chip
Minimize traumatic surgery	Avoid incapacitating or killing the subject
Small package	Unaffected by skull's curvature
Minimize mechanical stress	Prevent damage to brain
Use inert materials	Prevent damage to brain
Protect against infection	Prevent damage to brain or to the subject
Be immovable and stable	Prevent damage to package or to subject

requirements primarily insure survival of the subject and the chip. All of these requirements are met with the final design of the package. This design is presented in the next section.

Design of the Package

Using the requirements above, a package has been designed and fabricated. The design of the package is similar to a package presently used by the Wright-Patterson Air Force Base Aerospace Medical Research Laboratory (AMRL). The package which AMRL now uses consists of a cylinder permanently attached to the skull of a rhesus monkey. Through a hole in the cylinder, technicians can insert a wire probe down into the brain. When not in use, a teflon screw is inserted into the cylinder to prevent infection. This three part system of receptacle, probe, and protective sealant, forms the basis of the design used in this thesis. It consists of a three part package: the mount, implantable package,

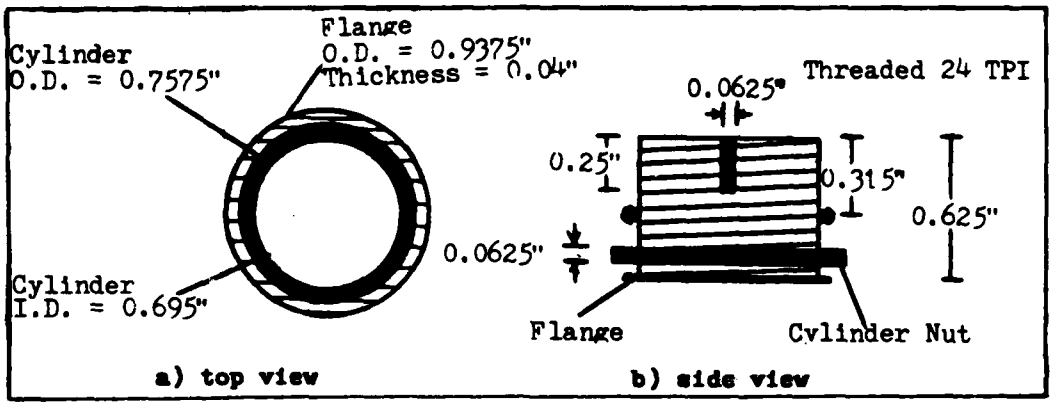

Figure 3. Brain Chip Package Outer Cylinder (Mount)

and protective cap. The complete package is fabricated from medical grade stainless steel and meets all the design requirements.

Mount. Like the AMRL package, the mount consists of a hollow cylinder which is to be permanently attached to the skull. This mount is designed to accept a cylindrical package which can be inserted directly onto the brain. The mount consists of two separate pieces: the outer cylinder (Figure 3) and outer cylinder nut (Figure 4).

The outer cylinder consists of a slotted, threaded cylinder with a flange protruding from the base. The inner diameter of the cylinder is 0.695 inches, with a wall thickness of 0.0625 inches. A flange, 0.0625 inches wide, extends the outer diameter of the bottom of the cylinder to 0.945 inches. This flange, which rests beneath the skull when in place, is 0.04 inches thick. Its purpose is to prevent the mount from being pulled out of the skull. The cylinder's length is 0.625 inches with two small threaded holes for set screws 0.315 inches from the top. The set screws hold the cylindrical package, when inserted, in place.

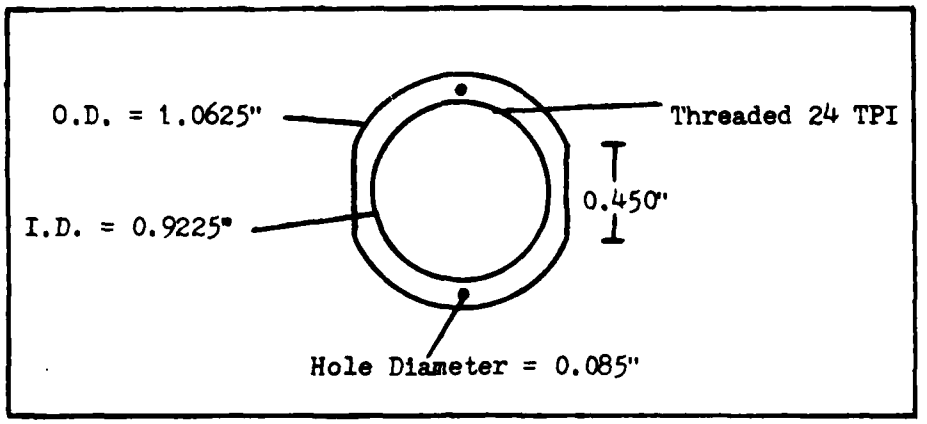

Figure 4. Brain Chip Package Outer Cylinder Nut (Mount)

Beginning at the top of the cylinder, a 0.085 inch wide slot is cut through the wall of the cylinder, down 0.250 inches. This slot prevents the cylindrical package from twisting when in the mount. The surface of the outer cylinder is threaded to accept the outer cylinder nut.

Threaded to screw onto the outer cylinder, the outer cylinder nut (Figure 4) is a 0.0625 inch thick, 0.140 inch wide ring measuring 1.0625 inches from side to side. With the outer cylinder's flange beneath the skull, the outer

cylinder nut is tightened down to the surface of the skull, locking the mount firmly into place. To aid in tightening the nut, opposite sides of the nut have been shaved off providing a 0.450 inch flat edge for a wrench to grasp. In addition, two 0.085 inch holes have been drilled on opposite sides to allow tightening with a tweezer-like tool. These holes are located 90° around the nut from the flat edges.

Implantable Package. Whereas the mount is permanently attached to the skull, the implantable package is easily inserted and removed. The

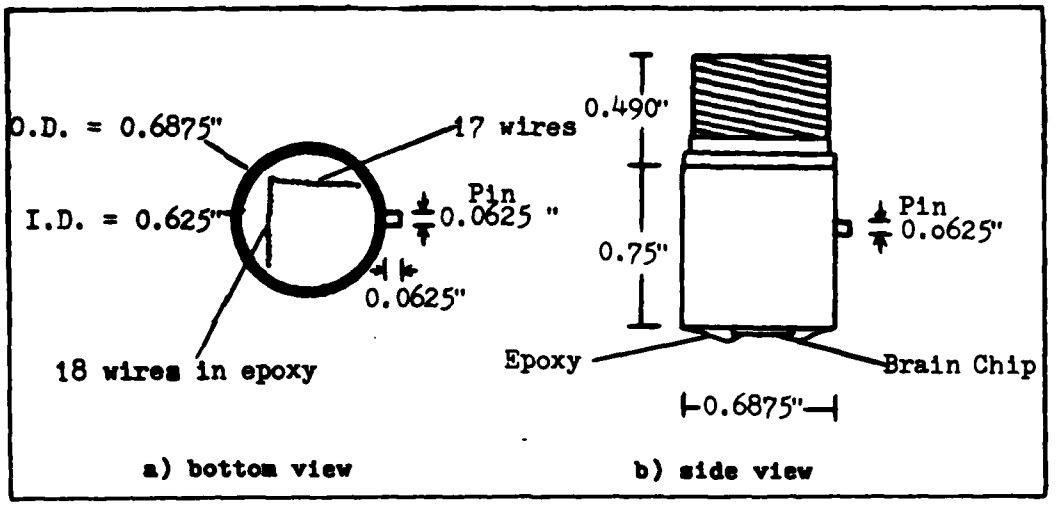

Figure 5. Brain Chip Package Inner Cylinder (Implantable Package)

implantable package, shown in Figure 5, is the inner cylinder of the brain chip package. As explained in the next section, this cylinder holds the brain chip on the bottom and the wire connector at the top. It consists of a 0.750 inch long hollow cylinder with a pin extending 0.0625 inches from the surface. The pin, a 0.0625 inch diameter solid wire, is centered 0.275 inches from the top. When the inner cylinder is inserted into the mount, this pin slides into the mount's slot to prevent twisting. The 0.250 inch depth of the slot allows the inner cylinder to protrude approximately 0.010 inches past the bottom of the mount, if needed. The inner cylinder is a thin-walled cylinder, with an inner diameter of 0.625 inches and an outer diameter of 0.6875 inches. This allows it to fit snugly into the outer cylinder.

Protective Cap. To seal the the package when the monkey is not being used for experimentation, two protective caps are required: one for the mount only and one for the mount with the implantable package.

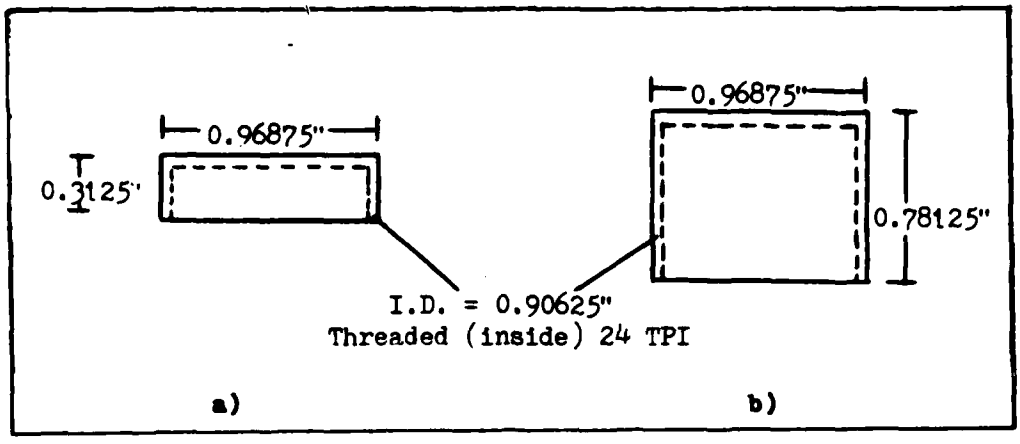

Figure 6. Protective Caps: a) without inner cylinder; b) with inner cylinder

The mount's protective cap (Figure 6a) is a 0.350 inch long cylinder, 0.96875 inches in diameter, sealed on one end. The inner wall of the cylinder is matched to fit the mount's threads. A rubber washer should be used inside the cap to provide a good seal. A 0.090 inch diameter hole should be drilled 0.10 inches from the bottom for insertion of a set screw. This cap is used when the inner cylinder is not inserted.

When the inner cylinder is in place, the cylinder and connector on top protrude 0.500 inches from the top of the mount. The cap described above, then, is too short for this combination. Therefore a similar cap, with equal diameter but measuring 0.78125 inches long is required as shown in Figure 6b. A rubber washer must be pushed down the connector and inner cylinder, to the top of the mount, to serve as a seal. A 0.090 inch diameter hole should again be drilled 0.10 inches from the bottom, for a set screw.

Design Requirements. The package described above meets the design requirements as stated in the prior section. The use of a permanent

mount with removable inner cylinder easily allows chronic implantations of the package without the use of surgery. The only required surgery is to place the mount into the skull. The package is small, though a smaller package would be desirable. Mechanical stress to the brain is avoided by the mount's slot and the inner cylinder's pin. No twisting of the package can occur once it is inserted into the mount, and the package cannot be pushed onto the brain. Since the whole package is made of medical-grade stainless steel, it is inert to the brain. As will be seen in the next section, the base of the inner cylinder will be coated with polyimide, which is also inert. The use of protective caps will help prevent infection, however, while in use, there will be no protective cap. At this time, chance of infection will be present. Finally, the mount is designed to remain in place. The flange beneath the skull and the nut above the skull lock the mount in place. During actual surgery, a procedure using dental acrylic will cement the mount in place, further immobilizing it. This package has been fabricated as designed.

Integration of Array and Package

Before the package can be used, the brain chip array and package must be integrated into an implantable device. This integration requires attaching the chip to the underside of the inner cylinder, running wires through the cylinder, attaching the wires to a connector, then affixing the connector to the top of the inner cylinder. The specific order for this is: preparing and attaching the wires to the cylinder, attaching the chip, and attaching the connector.

Preparing and Attaching the Wires. The purpose of the wires is to

allow external control and output from the chip. These wires must be attached to the chip on the bottom of the implantable package and the connector on the top (see Figure 5b). Epoxy is used to cement the wires into place in the lower half of the implantable package. Since the wires must be bonded to the chip, it is best to put the wires in a known order prior to epoxying them in. 30-gauge solid copper hook-up wire was chosen with kynor insulation, rated at 125° centigrade. The temperature rating is important, since these wires will be subjected to 180° centigrade during processing. Teflon coated wire would be better, but none was available. Thirty-five wires are used to allow essential connections, as well as testing connections. Appendix C contains a wiring diagram for the chip.

Prior to epoxying the wires in place, they should be ordered and numbered. One set of eighteen and one set of seventeen 2-inch long wires are tagged at one end with labels numbered consecutively 1 through 35. The wires in each set are straightened and placed side by side on a piece of masking tape (sticky side up) to hold them in place. When the set of wires are in place, the tape should be wrapped over the top to hold them in place. The tape should be attached to both ends of the wire to insure they stay ordered, and in place. The result is a flat line of wires.

To hold the wires in place in the cylinder, fabricate a thin cardboard (or stiff paper) insert to fit inside the cylinder. First cut a 5/8-inch circle from the cardboard, then cut slits for the taped wire packages so the two sets of wires will meet at a right angle, as in Figure 7. Allow enough room for the chip to lie within the vertex of the wires. Slip the wire packages into the cardboard slits, and slide

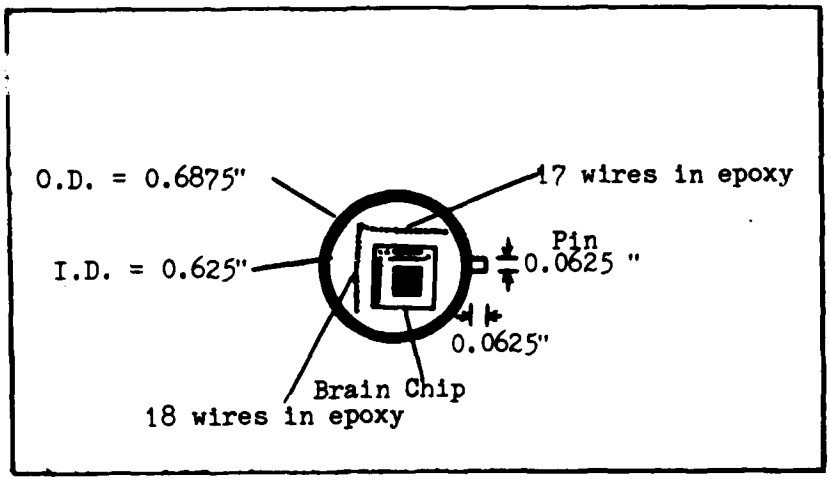

Figure 7. Inner Cylinder with Wires and Chip Attached (bottom view)

the insert into the inner cylinder. The insert should sit about 1/8-inch from the bottom. The wires should extend at least 1/4-inch beyond the bottom of the cylinder through the insert. Remove the tape from the bundle of wires between the insert and the edge of the cylinder's base to allow the epoxy to contact each wire. The wires should extend through the top of the cylinder with the labels visible.

With the wires and insert in place, the cylinder is ready for the epoxy. The epoxy should be capable of withstanding high temperatures. EpoTek H70E epoxy, produced by Epoxy Technology Inc., initially proved adequate for this purpose. A thin layer of epoxy should be spread around all edges of the cardboard insert and around the wires, then cured. This permanently cements the insert into the cylinder and seals all holes, preventing leakage of epoxy through the insert. After the holes are sealed, pour epoxy to fill the bottom of the cylinder, and cure according to the manufacturers cure schedule.

When completely cured, snip off the wire ends extending through the

epoxy, then sand the bottom of the cylinder to get a smooth surface. This should leave only smooth copper circles showing in the epoxy. These circles will be ultrasonically bonded to the chip.

Attaching the Chip. After the wires are in place, an encapsulated brain chip, described in Chapter III, is taped to the epoxy on the bottom of the inner cylinder. A piece of double-sided tape, cut to the same dimensions as the chip, is affixed within the vertex of the two sets of copper circles (wires) showing. The chip is then attached to the tape so that the output pads (see Figure 1) lay next to one set of wires , and the control circuit pads lie next to the other set (see Figure 7). Using an ultrasonic bonder, bond wires from the chip to the copper circles in the epoxy, noting the wire numbers for each pad. The bonding diagram used for this thesis appears in Appendix C. Before putting any protective coating on the wires, check the functionality of the chip's control circuitry, using a similar test set-up as in Chapter IV.

The bottom surface of the inner cylinder is now ready for its protective polyimide coating. To protect the fragile bonding wires, epoxy should be used to form a tough, protective layer. Use the same epoxy as for cementing the wires since it will also undergo high temperatures. The epoxy is necessary prior to the polyimide coat due to the shrinkage of polyimide as it cures. This shrinkage will break the wires, as shown in the references (see 11:6) and in testing in Chapter III. Apply the epoxy at the base of the wires, then build up to cover all bonding wires. Keep the build-up to a minimum as well as away from the electrode array. After curing the epoxy, thoroughly clean the bottom surface of the cylinder to remove all grease and ionic

contaminants. Use a procedure similar to the standard clean shown in Appendix A.

On the clean chip and cylinder surface, puddle VM-651, Polyimide Adhesion Promoter by Dupont. Let it sit for five seconds, then blow dry with N_2. This insures good adhesion of the polyimide layer. Apply the polyimide, by hand, across the surface of the cylinder, and over all epoxy on the chip. Insure all exposed metal pads are covered, except for the exposed electrode array pads. Cure the polyimide in stages to ease the strain caused by shrinkage. Use the following times and temperatures for best results: 70° C for 30 minutes; 120° C for 30 minutes; 150° C for 30 minutes; and 180° C for two hours.

Attaching the Connector. With the inner cylinder coated and wires attached, only the addition of a connector is required. The connector used in this thesis is an 85-pin microminiature connector from ITT Cannon Electric (see Appendix D). The preferred connector a 55-pin connector from the same company, was not available. However, the two are similar in size, and interchangeability should pose no problems. Details on the two connectors can be found in Appendix D.

Prior to using either connector, the unneeded wires should be trimmed off, and the other wires shortened to approximately 1/2-inch. The receptacle portion of the connector comes with a square mounting plate which must be shaved off using a lathe. The connector must be round to allow the protective cap to fit over it.

Using the bonding diagram, solder the wires from the chip to the wires on the connector, noting the pin number for each on the diagram. Since, the wires are to be pushed into the cylinder, each solder joint must be strong and well insulated. A silicone rubber sealant (RTV) is

recommended. Apply the RTV to each joint, and allow to cure overnight. After it cures, carefully push the wires into the cylinder, and affix the connector to the top of the cylinder. RTV was used to attach the cylinder in this thesis, only because removal may be required. Once more connectors arrive, they should be affixed to the cylinder with epoxy and cured at low temperatures to avoid melting the RTV or connector wires.

This completes the integration of the chip and package. All requirements for the package and chip are met in this integrated package. The polyimide covering insures that no reaction occurs between the CSF and epoxy, as well as sealing the inner cylinder.

Suggested Implantation Procedure

The integrated package is fully capable of non-surgical insertion into and removal from the brain. However, one surgical operation must be accomplished to implant the package's mounting hardware into the skull prior to use. Hensley and Denton recommended a procedure which is similar to that now used by the AMRL at Wright-Patterson AFB (5:102-103). AMRL's procedure is used to implant a stainless steel cylinder, similar to the implantable brain chip package, into a rhesus monkey's skull for the purpose of observing oxygen in the brain. The surgical procedure described below closely copies AMRL's techniques. For a detailed description of this procedure see references 4 (pages 76 - 81) and 15.

The outer cylinder (mount) and protective cap may be sterilized by either a hot or cold sterilization, since there are no sensitive parts associated with either. The monkey should be anesthetized using the

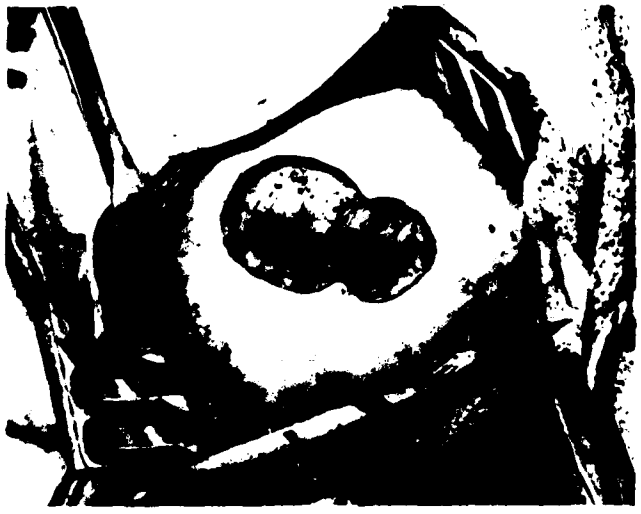

Figure 8. Surgical Cuts into Skull for Mount

schedule described by Hensley and Denton (5:76). After aseptically cleansing the skin covering the monkey's visual cortex region, the skin should be cut and pulled back to expose the skull.

A set of holes, similar to a keyhole, should be cut through the skull as in Figure 8. The smaller hole must be placed directly over the visual cortex, as this is where the mount and chip will sit. This hole must be semicircular with a diameter no less than 0.76 inches, and no more than 0.85 inches. The small hole is large enough to allow the cylinder to fit snugly, with the flange at the base of the cylinder beneath the skull. Under no circumstances should this hole be larger than 0.85 inches, or it may be possible for the flange to be pulled through the hole. If the hole is smaller than 0.76 inches, the outer cylinder will not fit into the hole. The larger hole should be slightly larger than 0.95 inches in diameter extending into the semicircular hole as shown in Figure 8.

After cutting the holes, the mount, with the cylinder nut threaded

Figure 9. Aerospace Medical Research Lab Implant Installed in Skull of Rhesus Monkey

up 1/4 inch from the base, is set into the large hole. The protective cap should be in place on top of the mount at this time. Insuring the flange stays below the skull and the cylinder nut above, the mount is slid into the smaller hole. While holding the mount in place, thread the nut down tightly against the skull, using a wrench or pair of tweezers. This will pull the flange up against the underside of the skull, and lock the mount in place. The large hole should be covered with bone wax, to reseal it. The installed package will look similar to the AMRL implant shown in Figure 9.

Dental acrylic will be used to cement the mount into place, as discussed by Hensley and Denton (5:78). First, use a dental burr to rough the surface of the skull around the mount. This allows the dental acrylic to adhere better to the surface. Place anchoring screws into the skull, approximately 0.20 inches from either side of the mount (see Figure 9). Spread the dental acrylic over the base of the mount, cylinder nut, roughed area of the skull, bone wax, and the anchoring screws.

This serves to permanently affix the mount, while sealing the holes in the skull. The skin should be returned to its original position around the base of the mount.

The mount is now ready for use. The inner cylinder should be inserted only when the monkey is restrained. The monkey can easily reach the mount with hands and feet. Therefore, when using the implantable device, a collar should be placed around the monkey's neck, wide enough to prevent it from reaching up. This should prevent the monkey from grasping any wiring.

This concludes the complete design of the implantable package. This package will meet all the requirements set out above. The suggested surgical procedure, although not a detailed description, serves as a guide to implanting the device securely into the skull. Most important, this design and surgical procedure produce a system which is safe, durable, and reuseable.

III. Encapsulation of the Array

The most important aspect of this thesis effort is protection of the brain chip from the corrosive environment of the brain. The encapsulating material, Polyimide 2555, must protect the chip's control circuitry from moisture and ion penetration. At the same time, the 16 X 16 electrode array must remain exposed to allow monitoring of the signals from the brain. Each electrode serves as the source of an adjacent NMOS transistor. The gates of these 256 transistors will quickly short in the presence of sodium ions, despite their silicon dioxide passivation layer. Therefore, a photolithography process must be used to expose the 256 electrodes, while covering their associated transistors.

In the attempt to encapsulate the chip, two photolithography processes were tried: positive and negative. Prior to using these processes on the brain chip, three-inch practice wafers were used to establish a consistent processing schedule which provided satisfactory results. After establishing the process with wafers, processing with individual chips was accomplished. The small size of the chips resulted in further refinement of the wafer process. Finally, the 16 X 16 electrode arrays of four brain chips were coated with silver, since the aluminum electrodes may react with sodium ions in the brain.

Practice With Wafers

Due to the limited number of brain chips available and the difficulty in working with individual chips (measuring 9/32 inches on a side), three-inch practice wafers were used to establish an encapsulation

process. These practice wafers contained only a silicon dioxide layer. The three-inch wafer size was chosen since the mask aligner used that size.

Initially, positive photolithography was attempted. This process was chosen over the negative process due to its simplified develop/etch method. Positive photoresist (PR) develops with a basic chemical, such as AZ351. Polyimide etches with a basic chemical also. Therefore, only one chemical is required with the positive photolithography process. With the negative process, three separate chemicals are required. In addition, positive PR can be stripped easily with acetone, without affecting the polyimide layer. Standard negative PR removal requires use of harsh stripping agents which can remove the polyimide finish also (6:21).

However, positive photolithography did not produce satisfactory results. Therefore, negative photolithography was attempted and found to produce satisfactory, repeatable results. A list of the chemicals used during the photolithography process, as well as their manufacturers, can be found in Appendix B.

Positive Photolithography

The positive photolithography process initially attempted, was derived from La Voie's thesis (6:21 - 22) and actual experimentation. First, a standard positive photoresist application and developing schedule, without polyimide, was established. A number of three-inch wafers were cleaned and dried according to the Standard Cleaning schedule in Appendix A. Applying both the HMDS (positive photoresist adhesion promoter) and AZ1350J (positive photoresist) as per the Positive PR

Process for Wafers (Schedule #1, Appendix A), only the exposure time and development schedule were varied.

Exposure times less than 20 seconds normally resulted in a well defined pattern, but it would not develop all the way through to the silicon dioxide layer. Exposures up to 60 seconds appeared normal when developed, but edges did not seem as sharply defined. An exposure time of 20 seconds was decided upon, due to its ease of develop and sharp pattern all the way down to the silicon dioxide layer. The develop portion of the schedule was similar to La Voie's, and gave consistent results (6:13).

With establishment of a standard schedule for use of positive PR, work began on using this process over a polyimide layer. The polyimide used was PI-2555 by Dupont (see Appendix B). In its original form, PI-2555 is a polyamic acid solution which converts to polyimide when exposed to heat (16:1). To enhance adhesion of the polyimide layer to the wafer, Dupont recommends use of its adhesion promoter, VM-651, before applying the polyimide. The VM-651 must be reduced by adding one drop of VM-651 to a 200 ml mixture of 95% methanol and 5% deionized water (DIW). This solution must normalize for 12 hours prior to use, then be discarded after 20 days (16:1). Hensley and Denton did not use this adhesion promoter in their work. However, La Voie found that adhesion is definitely enhanced (6:61-67) and pinhole defects reduced (6:43) when the VM-651 is used.

All runs with polyimide (both positive and negative), used steps 1 through 9 exactly as outlined in Schedule #2, Appendix A. This part of the schedule duplicates the schedule used by La Voie (6:21-22). Except for one wafer, all runs used unthinned polyimide to obtain maximum

thickness. The thinned polyimide run (thinned 4:1 PI 2555 to Dupont T-9035 Thinner) resulted in an unusually large number of pinhole defects. This agrees with La Voie's results in pinhole defect tests (6:49-51).

In an attempt to obtain satisfactory results, some variations were made in steps 10 through 18. Unfortunately, none of the variations were completely successful. Nearly all runs resulted in uneven develop/etch rates across the wafer. This is due to the AZ351 being both developer for the positive PR and etchant for the polyimide. As the AZ351 develops through the PR, it begins etching the polyimide. Therefore, when the pattern is fully developed, some (but not all) of the polyimide has already been etched.

In a similar manner, when the polyimide is etched, the AZ351 continues to destroy the PR layer. This results in photoresist lifting and deterioration of the pattern. La Voie had similar difficulties with the uneven etch rates.

In an attempt to balance out the etch rates of the develop and etch processes, a number of steps were varied: PR develop time, postbake temperature, etch time, and type of etchant. The photoresist develop times were varied in an attempt to get a fully developed pattern without etching the polyimide. Times as low as 15 seconds of AZ351 resulted in sharp, barely visible patterns. Additional develop time etched holes in the exposed polyimide, randomly across the wafer, as well as blooming of the pattern edges (overdeveloped). This occurred whether the wafer was developed on a spinner (at 1 krpm) or in an AZ351 bath.

To prevent overdeveloped patterns, a minimum develop time was tried. This was followed by a postbake to harden the photoresist. The

temperature ranged from 70° C for 30 minutes to 150° C for 30 minutes. In the case of the lower temperature, there did not appear to be any difference in the ability of the PR to stand up to the etch. At 150° C, neither the polyimide nor PR could be etched. A compromise temperature of 100° C for 20 minutes showed the most promise, but it was still impossible to etch the polyimide without lifting off the photoresist first.

The postbake toughened up the polyimide, requiring an increased etch time. Some etch times over seven minutes long had no effect on the polyimide after a 100° C postbake. Different polyimide etching solutions were also attempted. Various concentrations of AZ351 and NH_4OH (ammonium hydroxide), ranging from full strength to a 10:1 mixture, were used also. The full strength etchants normally etched at the expense of photoresist pattern. The weaker etchants would not etch.

After repeated failures, the positive photoresist process was abandoned. It appears the weak link in the process is the positive PR. It is impossible to toughen the positive PR without also toughening the polyimide. Therefore, any etchant that affects the positive PR will destroy the pattern as it etches the polyimide. However, one step not varied was the exposure time. The exposure time was based on the initial photoresist-only wafers. The exposure time is related to the reflectivity of the wafer's surface. A decrease in this reflectivity, such as adding a polyimide layer underneath would cause, may require a longer exposure time. This longer exposure will weaken the PR in those areas to be etched, at least allowing an easier develop. However, there is no insurance the PR will still be capable of withstanding the

etchant. Therefore, an alternative process, negative photoresist, was attempted.

Negative Photolithography

Since Hensley and Denton had proven the success of negative PR, this method was used next. The schedule developed for this process was based on both La Voie's work (6:17:18) as well as that of Hensley and Denton (5:C-1 - C-2). All practice was done using both polyimide and negative PR to obtain Schedule #3 of Appendix A. The primary difference between the negative and positive photolithography processes is the chemicals required for developing. While the developer of the positive process also etches the polyimide, the negative PR developers have no affect on the polyimide. Therefore, the etching process is independent of the developing process.

Cleaning, application of the polyimide coating, and prebake procedures remained exactly as in the positive PR schedule. The negative photoresist application schedule remained constant with all the 3-inch wafers tested, but the exposure times, develop times, postbake time and temperature, and etch times were varied.

Negative photoresist exposure times are normally much less than those used with positive photoresist. The time exposed to ultraviolet light ranged from 2 to 10 seconds. The greater the exposure time, the tougher the PR. The 2 second exposure resulted in a well defined pattern, but it lifted and wrinkled during etching. Times of 4.5, 8, and 10 seconds all had good results. The 4.5 second exposure time was chosen since it had proven successful for Hensley and Denton.

The developers used on the negative PR were xylene (for develop)

and butyl acetate (for stop). The variations of the develop times ranged from 20 to 35 seconds of xylene. Both spinning and bath methods were used. All times resulted in acceptable patterning, but those developed for longer periods were more easily undercut during the etching process. Using the spin develop method for 20 seconds gave an excellent pattern which appeared to "V" in toward the center. This pattern was not as severely affected by undercutting.

Variations of the postbake time and temperature ranged from no postbake up to 120° C for 20 minutes. With no postbake, the PR was vulnerable to undercutting during etching. Both 100° C and 120° C postbakes had satisfactory results, with the higher temperature showing a higher resistance to damage during etching.

The most difficult time to optimize is the etching time. The etchant used was AZ351 mixed as in the positive photolithography process. The etching time necessarily varies as the other steps in the photolithography process vary. A low exposure time or high develop time could result in a weakened PR layer, necessitating a smaller etch time. Higher postbake times and temperatures toughen not only the PR layer, but the polyimide layer, too. This requires a longer etch time. Normally, over-etching will cause an undercutting as the etchant removes polyimide beneath the PR layer, without harming the the pattern. If the undercutting becomes too extensive, the PR layer can tear away. Etch times began as low as 3 seconds. This amount of time was never enough to fully etch, but allowed an estimation of additional etch time after observation under a microscope. Under most variations, a 5-second etch had the best results.

Upon obtaining a satisfactory, repeatable schedule, its ability in

Figure 10. Results of Applying Polyimide to an Uncured Surface

processing additional coats was determined. The negative PR layer was not removed from the polyimide layer because it would probably remove the polyimide layer also (6:21).

Prior to adding another coat, the polyimide was cured using the same time and temperature as Hensley and Denton: 120° C for 20 minutes. This was done immediately after etching. After removal from the oven, the adhesion promoter and polyimide were applied as usual, with unexpected results. The photoresist layer was completely washed from its pattern and scattered around the wafer. Further testing on an identically prepared wafer showed that even a drop of polyimide on the postbaked PR/polyimide surface caused cracks throughout the pattern, as shown in Figure 10. The cracks were in the postbaked polyimide layer beneath the PR. The PR layer on the first wafer had washed away due to extensive cracking of the polyimide below it. It appeared a final cure was probably required prior to an additional coat of polyimide. Using

a 180° C cure for 2 hours, a second coat was successfully applied.

Individual Chips

After establishing the schedule for 3-inch practice wafers, it was applied to the individual chips. However, after applying the practice schedule to a number of chips, it was evident that some modification was required. The size of the chips introduced new problems which were eventually overcome. Additionally, a method of removing the PR between layers was found. Some of the problems required modifications to equipment. These will be discussed in Chapter V.

When Schedule #3 (Appendix A) was applied to a single chip (measuring 9/32 inches by 9/32 inches), it failed to produce a satisfactory developed pattern or an acceptable etch. The first problems noted were in the initial layer of both the negative PR and the polyimide. A significant build-up, a meniscus, occurred on the edges of the chip. This happened with both the polyimide and the PR. A slower spin speed during application of the polyimide thickened the meniscus, while a faster speed resulted in a very minor reduction of it. The PR was affected similarly, but its thickness was much more noticeable. This may have been due to a compounding affect from the polyimide meniscus. There did not appear to be any way to eliminate this meniscus, and it was the probable cause of the abnormally developed pattern of the PR.

When the PR was developed, a bubbling occurred throughout the layer. This bubbling was most pronounced on the edges of the chip, where the meniscus occurred, as can be seen in Figure 11. However, bubbling also appeared randomly across the chip. Initially, it seemed the polyimide was being affected by the developing chemicals. Further

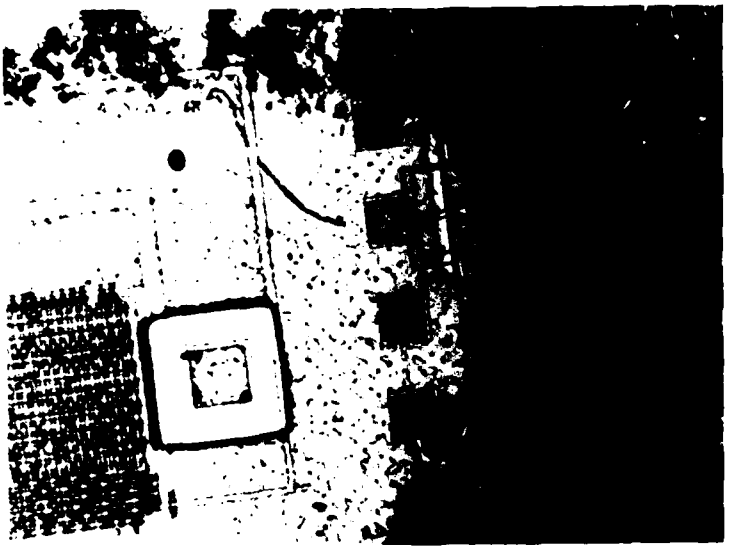

Figure 11. Bubbling Effect on Edge of Chip During Developing

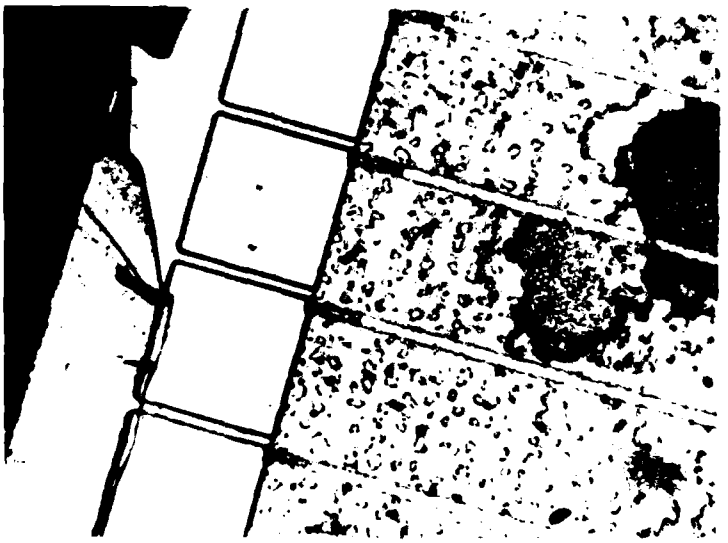

Figure 12. Tearing of Negative Photoresist Pattern on Edge of Chip

tests showed the bubbling was restricted to the PR material only; the polyimide layer was intact. As these chips were etched, the PR pattern would tear away on the edges, while the interior pattern etched normally (see Figure 12). Since the bubbles occurred primarily on the edges,

it was felt the meniscus was responsible. It appeared the thickness of the meniscus prevented a satisfactory drying of the PR as well as allowing the developing chemicals to enter under the outer edges, weakening the PR. When etched, the weakened PR would then give away.

To obtain better results, it was obvious the effects of the meniscus must be reduced. Increasing spin speed was not enough. In an attempt to break down the invisible barrier holding the polyimide to the edge (surface tension), polyimide was puddled on the chip until it flooded over the edges onto the spinner's chuck holding the chip. This broke the barrier and significantly reduced the meniscus. This procedure was also followed with the negative PR. In addition, the spin speed and prebake temperature were increased for the PR. The increased speed slightly reduced the PR thickness, and the increased temperature during prebake insured the PR was thoroughly dried. When the chip was developed, there was no longer any bubbling effect. A slight defect occasionally appeared on the edges, but the increased prebake temperature strengthens the edges and a decrease in develop time prevents a weakening of the PR.

The developed pattern was now acceptable, but a problem existed with the etching process. Due to the postbake, the polyimide required at least 8 seconds to etch fully. This length of time often undercut the pattern. The polyimide seemed to be toughen more than the PR pattern during the postbake. The postbake was dropped and the etch time decreased. The result was an excellent pattern which stood up to a full etch.

The revised schedule produced multiple layers of polyimide with excellent results. However, the negative PR layer, with its occasional

defects, remained between each layer. During a cleaning of an encapsulated chip, it was discovered that light scrubbing with acetone would removed hard baked negative photoresist without damaging the polyimide. As long as the polyimide had cured for 2 hours at 150° C, the PR could be stripped successfully. This was incorporated into the revised schedule which appears as Schedule #4 in Appendix A.

Addition of Silver Electrodes

A properly encapsulated chip will protect the chip's circuitry from the CSF. However, the exposed portions on the chip, the aluminum electrode pads in the array, may react with the saline environment, possibly affecting the brain's normal functions. Therefore, a method of protecting the brain from the aluminum pads was needed. The solution was to cover the pads with a material often used in vivo: silver.

The addition of silver on aluminum is common in fabrication of integrated circuits. However, this is usually done during manufacture of the circuit. This metallization process consists of using photolithography to develop a pattern in a photoresist layer on the IC, then, in a vacuum, evaporating the metal onto the surface. The photoresist is then stripped, leaving the metal only in the exposed pattern. The wafer must then be annealed at 450° C to set the metal permanently into the IC. When using both aluminum and silver, the aluminum is evaporated first, followed by the silver. This is done without breaking the vacuum in the evaporator to prevent the growth of an oxide on the aluminum (aluminum oxide).

Since the brain chip already contains aluminum pads, an attempt was made at adding silver only to the pads. The only concern was the

pre-existing aluminum oxide coating on the pads. The aluminum oxide serves as an insulator and may prevent the silver from contacting the aluminum. Although the oxide could be removed, this could not be done in the same vacuum as the metallization was to be done with the equipment available. If done outside the vacuum, the layer would grow back before a vacuum could be established. However, discussion with Mike Sopko, who was fabricating a JFET version of this chip in a related thesis (reference 17), led to the belief that silver would migrate through the oxide into the aluminum, especially during the anneal.

Schedule #5 in Appendix A was used to apply the PR to the chip. Positive PR was used since it is easy to remove after metallization with little effect on the metal. The schedule was developed from discussions with Sopko, since he used positive PR exclusively throughout his fabrication process. Two chips were patterned using Schedule #5, then placed into the evaporator. A 1500 angstrom layer of silver was deposited on the aluminum pads. However, when the PR was stripped, all of the metal lifted. The silver apparently would not attach onto the aluminum oxide.

A second attempt was made at metallization. In this attempt, both aluminum and silver would be deposited, as is usually done in fabrication. Since aluminum oxide readily attaches itself to aluminum, it was felt that deposited aluminum would attach itself to the oxide. This new layer of aluminum would then accept the silver.

Four chips were prepared using Schedule #5, then placed into the evaporator. After establishing a vacuum, 1000 angstroms of aluminum were deposited, followed by 1500 angstroms of silver. These thicknesses were the same as those used by Sopko in his thesis. When the PR was

removed, the metal remained. An anneal at 500° C for 10 minutes was done to set the metal, as well as drive the silver and aluminum into the original aluminum pads.

The addition of silver appears to be successful. The only question that remains is the effect the aluminum oxide may have. Time prevented a test of the chips with silver electrodes to determine any additional impedance which may be present. If the aluminum and silver did not drive through the oxide, there will be a capacitive effect caused by the insulating layer. This should be tested in any follow-on work.

Integration of Array and Package

With successful encapsulation of the brain chip completed, it had to be packaged to test for its ability to protect the chip. Two types of packaging were accomplished for testing. The initial testing would be done in a 64-pin IC package due to the relative ease in constructing this type of package. The final testing, as well as the final product, would be in the package designed in Chapter II. Both types of packaging are described here. The actual testing is described in Chapter IV.

64-Pin Packaging. The 64-pin IC package was chosen as a package for the brain chip due to the number of pins available. The control circuitry on the chip must be bonded to the package to operate the chip. In addition, some electrodes, output columns, and row pads must be connected to allow monitoring of the chip for correct operation. However, none of the bond wires must cross the array if the package is to be tested in a saline environment. This is because all the electrodes must be completely exposed to the saline environment during the test. The 40-pin IC package does not allow this, but the 64-pin

package does. The specific wiring of the 64-pin package is not critical, but the following should be bonded to the package (refer to Figure 1):

1) GND - for input
2) PHI2 (Ø2) - to monitor 2-phase clock
3) PHI1 (Ø1) - to monitor 2-phase clock
4) CLK - for master clock input
5) SYI - for input (must be low for chip to work)
6) CS2 - CSØ - for count selector input
7) TS3 - TSØ - monitor counter/input count
8) CON - an input to control tri-state (TS) pads for input/output
9) SYO - to monitor synch out pulse
10) VDD - for input
11) ROWS - at least 4 rows (1, 5, 9, and 13) to monitor multiplexer output
12) OUTPUTS - as desired to monitor inputs to electrodes
13) ELECTRODES - at least one on each wired output column

After bonding the chip, it should be functionally tested, as in Chapter IV. The bond wires must then be protected prior to saline testing. Like the chip's circuitry, the wires and the pads they are bonded to must be protected from the sodium ions. This can be accomplished by spreading polyimide over the wires, package pads, and bonding pads, then curing it. However, the shrinkage rate of polyimide necessitates additional protection.

Polyimide has a high rate of shrinkage during the cure process. Thick coats, as those applied by hand, are capable of breaking bond wires (11:6). Different cure schedules were used in an attempt to minimize the effects of shrinkage. Emphasis was placed on slow cures, using 30 minute cures at 70° C, 120° C, and 150° C, prior to the 2 hour, 180° C full cure. However, all attempts resulted in numerous broken wires.

To prevent the polyimide shrinkage from breaking the wires, epoxy was applied to the wires. The epoxy was carefully potted on the pads,

then built up to cover the wires completely. Care was taken to prevent the epoxy from running onto the array. After the epoxy was fully cured, polyimide was applied by hand over it. A high temperature epoxy must be used, since the polyimide must be cured at 180° C.

The first epoxy used was a commercial brand readily available at drug stores. Rated at 300° F (150° C), it softened at 180° C, allowing the polyimide to break the wires. However, the second epoxy, EpoTek H70E, seemed to remain solid during the polyimide cure, holding the wires in place.

After the polyimide (over epoxy) has fully cured, the package should be inspected to insure full coverage. All bonding pads on the chip and the package must be covered, as well as the epoxy. The 64-pin package is now ready for testing.

Implantable Device Packaging. Integrating the brain chip to the implantable package is not as simple as the 64-pin package integration. This is due to the number of wires in a small area (the cylinder). The wires must be bonded to the chip on one end and soldered to the connector on the other.

The implantable device is made basically from the design in Chapter II. The differences are in the preparation of the wires and the epoxy surface. Instead of labeling the wires with numbers, different colored wires should be used. The taped labels decompose at high cure temperatures, falling off the wire and leaving a sticky residue. The colors should be ordered in a recorded pattern to distinguish them from each other by color instead of numbers. After epoxying the wires in place, the bottom was sanded with four varying grits of wet sandpaper. The sanding was done with waterproof grits of 200, 220, 280, and 300.

The encapsulated chip was attached to the smooth surface, bonded, and protected with epoxy as described in Chapter II. The power/time settings on the bonder were 1.9/3 for the pads, and 5.0/3 for the kynor wire ends. The epoxy, as well as the polyimide, was applied while watching through the low-power ultrasonic bonder microscope. This enables precise application and enhances monitoring of possible broken wires. After curing the protective epoxy layer, the surface was cleaned and prepared for the polyimide covering to optimize the polyimide's adhesion. However, it appears the cleaning chemicals, as well as the adhesion promoter, react with the epoxy. Specifically, both acetone and methanol soften the epoxy surface, and it easily crumbles in places.

Since adhesion promoter is a 95% methanol solution, it has similar effects. Although a clean surface and adhesion promoter enhance adhesion of polyimide, these chemicals may weaken the epoxy layer over the bond wires and should not be used.

After the polyimide was applied and cured, the connector was attached to the wires. Since only one connector was available for this thesis, the wires were not shortened and the square mounting flange was not cut off. The connector was soldered using a low power soldering iron and a hea. sink on the chip wires. Care must be taken to match the correct brain chip wires to the correct connector wires. Using the colored wires aids in finding the right wires (see Appendix C). The soldered wires were insulated with black electrician tape.

At this point, an insurmountable problem was found. Most of the wires appeared to have broken their bonds. Although the EpoTek H70E can withstand temperatures as high as 300° C during wire bonding

operations, it is not rated for high temperatures over long periods of time. During the polyimide cure (180° C for 2 hours), many of the wires separated from their bonds beneath the epoxy. This was proven by bonding eight pins of an IC package to the L-BAR of a brain chip, then applying epoxy and polyimide as above. After curing the epoxy, only seven pins showed continuity, suggesting possible shrinkage of the epoxy. After fully curing the polyimide, only four pins still showed continuity. This problem is insurmountable only in this thesis due to lack of time. An epoxy capable of withstanding the 2-hour, 180° C cure must be found, or another method of protecting the delicate bond wires determined.

IV. Testing of the Encapsulated Array

The purpose of the polyimide encapsulation of the array is to protect it from the corrosive, saline-like environment of the cerebrospinal fluid (CSF). Although polyimide has successfully protected an integrated circuit from the CSF (see reference 5), a new integrated circuit, new processing schedule, and new package are being used. Therefore, the polyimide encapsulation must again be tested to insure these changes have not affected the polyimide's ability to protect or the chip's functionality.

The 4 X 4 array, which did survive the CSF, uses JFET technology, and has silver electrodes. The 16 X 16 array is NMOS technology, and has aluminum contacts. Therefore, the ability of a polyimide-encapsulated NMOS circuit to survive the CSF must be tested. In addition, any variations in the chip's performance due to exposed aluminum contacts must also be ascertained.

The 4 X 4 array package consisted of a silicon square covered with polyimide. The new package contains the chip, epoxy, and polyimide, within a stainless steel cylinder. The ability of this new package to withstand the CSF must also be determined.

To accomplish the testing, a versatile test set-up was established. This set-up is used throughout most of the testing. Testing of the new brain chip is accomplished in two steps. Initial circuit testing is done in a 64-pin integrated circuit package. Final testing is then done in the implantable package described in Chapter II and Chapter III.

Test Equipment Set-up

The test set-up used in most of the testing allowed dynamic changes of the inputs as well as easy monitoring of the outputs. The equipment used included an elite board, an eighttrace oscilloscope, a sine-wave generator, and a simulated "brain". An additional test set-up, used for the final test, included external TTL circuitry to replace the chip's control circuitry.

Elite Board. The elite board was used to provide control connections to the "brain" chip, as well as points for monitoring the outputs. The board included a clock, variable from 10 Hz to 1 MHz, a +5 volt power supply, and four switches, allowing selection of +5 volts or 0 volts (GND).

The 64-pin package fit easily onto the breadboard strip of the elite board. Power, ground, and clock connections were made to the chip as described later in Circuit Testing. The clock was set to 1 KHz. Three switches were wired to the chip's count select inputs (CS0 - CS2), allowing easy change to these inputs. Wire leads were connected to most of the pins to allow easy access to the oscilloscope, for monitoring any of the signals. These leads were labelled with the function of the pin, enabling quick location of the various pins.

Oscilloscope. The oscilloscope used allowed monitoring of up to eight inputs simultaneously. Inputs were connected via coaxial cable with a BNC connector at the oscilloscope end and two clips at the circuit end. Normally, the counter outputs (TS0 -TS3), row outputs (ROW), and column outputs (OUTPUT) were monitored. In addition, sine wave input to the chip was also monitored.

Sine-Wave Generator. A Wavetek oscillator provided the sine wave

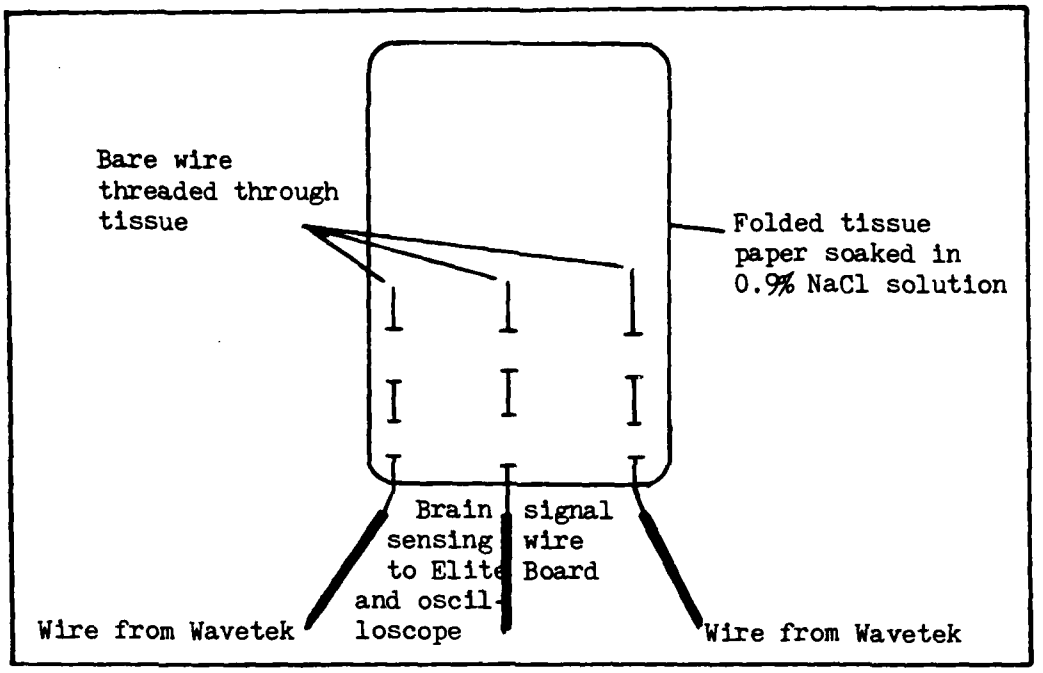

Figure 13. Simulated "Brain" Design

input to the chip. This input was variable from 0 Hz to 100 KHz. However, the frequency was kept between 1 and 5 KHz. The output of the Wavetek was input into the oscilloscope, the chip, and the simulated "brain".

Simulated "Brain". The simulated "brain" provided the test environment for in vitro testing. Its purpose was to closely replicate the corrosive environment of the CSF. The simulated "brain", shown in Figure 13, consisted of folded tissue paper soaked in a 0.9% solution of sodium chloride (NaCl). Leads from the Wavetek sine-wave generator were attached to opposite ends of the tissue, and a sine wave signal fed across it. An additional wire, attached to the center of the tissue, was connected to the oscilloscope to monitor the simulated "brain" signal. With a 26 millivolt peak-to-peak signal applied to the tissue, a 9 millivolt simulated "brain" signal was produced.

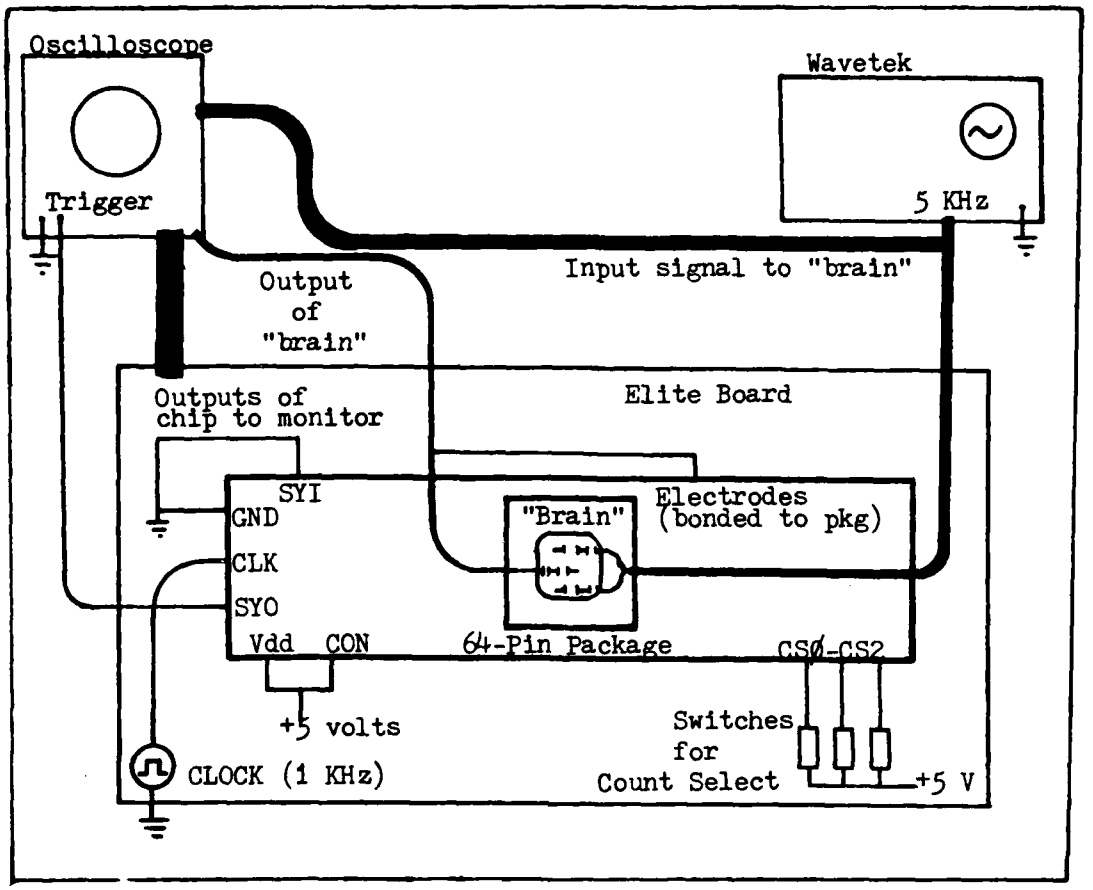

Figure 14. Test Equipment Set-Up

Equipment Integration. To form the test set-up, the elite board, with the brain chip in place, had to be connected to the oscilloscope, sine-wave generator, and simulated "brain" (see Figure 14). Only eight traces can be monitored at a time on the oscilloscope. However, the oscilloscope lead wires can be reattached to any of the chip's labelled lead wires at any time. The oscilloscope is used not only to sense the existence of a signal on a particular pin, but to measure its voltage and frequency as well. TTL voltages were measured on the 5 volts/div scale, while "brain" signal voltages were measured on the 0.02 volts/div scale (the minimum setting). On the minimum setting, noise

from the overhead fluorescent lights and the high capacitance of the oscilloscope resulted in difficulty reading the display. Therefore, to interface the chip's output signals to the oscilloscope, a 47 kilo-ohm resistor was inserted between each "brain" signal output pin and GND on the elite board. The oscilloscope is triggered by the synch out pulse, SYO, of the brain chip.

The Wavetek sine-wave generator has lead wires to both the oscilloscope and the simulated "brain". The simulated "brain" connection must remain throughout the test to drive the signals on the "brain", but the lead to the oscilloscopecan be disconnected. Its primary purpose is to adjust the output of the Wavetek prior to initiating the test.

The simulated "brain" must be connected to the Wavetek, oscilloscope, and the electrodes of the brain chip. The Wavetek provides the input, and the oscilloscope allows measurement and monitoring of the simulated "brain" signals. Connection between the brain chip and the simulated "brain" can be established in two ways: through a direct connection to any electrodes bonded to the 64-pin package, and through surface contact. The direct aids in verifying operation of the electrode circuitry without subjecting it to the possibly harmful simulated "brain". However, normal connection between the chip and simulated "brain" is through the actual contact of the simulated "brain" with the electrodes. This is accomplished by pressing the simulated "brain" into the well of the 64-pin package, or by turning the package upside down onto the simulated "brain".

Alternative Test Set-up. Due to the difficulty in fabricating a completely working package, an alternative test set-up was required to test the working portion of an encapsulated brain chip. Due to broken

wires inside the package, the control circuitry was completely inoperative. However, since the ROW and OUTPUT wires remained attached, the chip was still testable to some degree. Therefore, using TTL integrated circuits, a counter and multiplexer were designed to drive the functioning ROW signals. This external control circuitry consisted of one 74193 4-bit counter, one 74155 two-to-four decoder, one 7404 hex inverters, and one 7408 quad 2-input AND gates. The connections between these chips is shown in Figure 15. Only the two least significant outputs were used from the 4-bit counter, since only four ROW wires were used. The two counter outputs were input into the 74155 to decode one of four output lines. The outputs of the decoder remain high until one line is decoded. Since the decoded line transitions to a low, it must be inverted. Therefore, the decoder outputs are inverted in the 7404.

These inverted outputs are now counting pulses, similar to the outputs of the on-chip multiplexer. However, their pulse width is too long. Therefore, these pulses are ANDed with the external clock driving the counter. This clock's pulse width can be narrowed, giving distinct output pulses to the ROWs.

A different elite board was used in this test set-up. The clock on this board is adjustable in frequency, pulse width, and amplitude. The only circuitry on the elite board was the external control circuitry. The encapsulated brain chip was external to the elite board, and resided in a petri dish containing the simulated "brain". The interconnections between the brain chip package and elite board were to the ROW and OUTPUT leads on the package. As in the first test set-up, 47 kilo-ohm resistors were placed on the elite board from the OUTPUT connection to ground. With this alternate test set-up, a previously inoperative

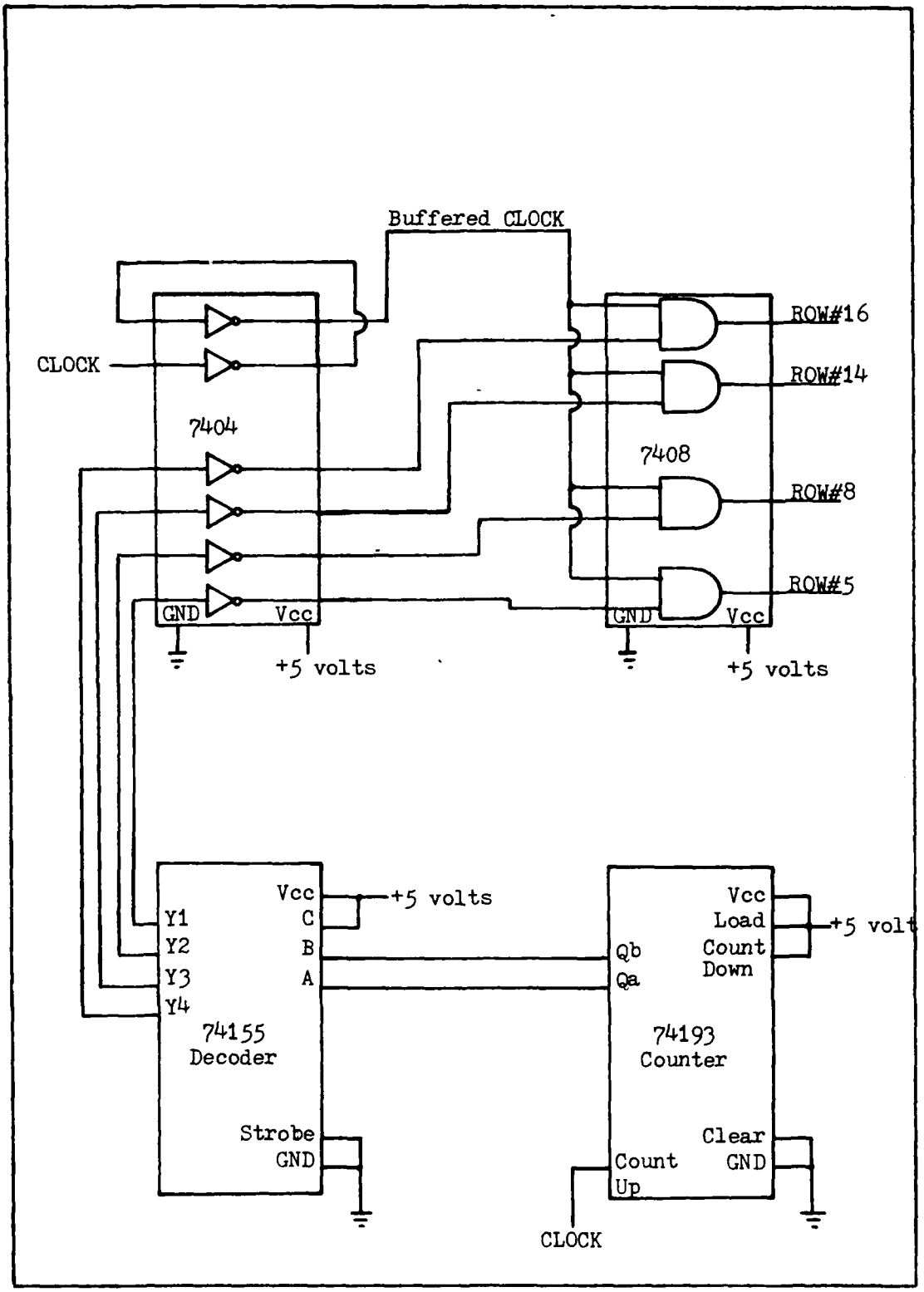

Figure 15. External Control Circuitry Design

brain chip array could still be tested.

Circuit Testing

Initial circuit testing was done in the 64-pin package due to the ease of fabricating such a package. The chip only needs to be bonded to the package and the exposed wire leads coated with polyimide. The purpose of this testing is to insure functionality of the chip in a saline environment. Tests in the 64-pin package were first run on unencapsulated array chips, then encapsulated chips.

Unencapsulated Array Test. An unencapsulated array was tested first. An unencapsulated, cleaned brain chip was fastened into the well of the package with double-sided tape, then wire leads were bonded from the chip to the package. These lead wires connected the control circuitry, the output pads, and some electrode contacts to the pins of the package.

The connected control circuitry included the following required connections (refer to Figure 1): VDD, GND, SYI, CLK, CON, and CS0 - CS2. In addition, other connections were made to allow monitoring of the control circuitry's operation. The two-phase clock outputs, O1 and O2, were bonded up to verify proper operation of the clock pad. The synch out pulse, monitored through SYO, was used to trigger the oscilloscope upon completion of each ROW count. To check correct operation of the counter, TS0 - TS3 were bonded. Finally, a representative number of ROW pads were bonded to check proper operation of the multiplexer output.

The other bonds between the chip and package were to a representative number of output pads and to a small number of electrodes in the

array. When a ROW pulse is high (+5 volts), any signal applied to an electrode in that row will appear at the output pad in the same column. The electrode, therefore, is the source of an NMOS transistor, the ROW pulse is the gate, and the output pad is the drain. Some of the electrode pads in the array were bonded to the package to allow an external signal to be injected into the array through the pins on the package. This helps insure proper operation of the transistors in the array without exposing the chip to the saline solution. Only electrodes on the periphery of the array were bonded to the package to prevent crossing other electrodes with wire. A complete wiring diagram of the unencapsulated array chip can be found in Appendix C.

After bonding the unencapsulated chip to the package, the fragile bond wires were completely coated, by hand, with epoxy. When cured, the epoxy protects the wires from the shear pressure caused by polyimide shrinkage during polyimide cure. However, the epoxy used in this thesis, Epotek H70E, was unable to withstand the high cure temperature of the polyimide, and allowed some wires to break at the bonds. Many of the wires did remain attached, though, allowing some testing.

When the epoxy was cured, the polyimide (PI 2555) was applied, by hand, over the epoxy and around the chip. Except for the electrode array and surrounding L-bar, the entire chip should be coated with the polyimide. This insures the sodium ions will not attack any part of the control circuitry or lead wires through the epoxy. The polyimide was cured using the following schedule: 20 minutes at 70° C; 30 minutes at 120° C; 30 minutes at 150° C; and 2 hours at 180° C.

The 64-pin package, with only the electrode array's drain-gate-source circuitry unprotected, is then inserted into the elite board.

The connections are made, as described earlier, except the simulated "brain" is not yet inserted into the well of the package. A functional test is accomplished to determine if any wires have broken, and how much of the control circuitry still works. This functional test checks the ability to change the counter output (TS0 - TS3) through different combinations of the count select inputs (CS0 - CS2). The occurrence of the ROW pulses changes as the count select inputs change according to Appendix F (page F-8). The ROW counts were checked to ensure that all sixteen rows could be turned on.

Four oscilloscope leads were then attached to the OUTPUT columns in which input source electrodes were bonded to the package. Setting up the simulated "brain" in a petri dish, the sensing wire to the oscilloscope is connected to the wired electrodes. The output of the wired electrodes should appear on the oscilloscope only when the associated ROW pulse is high.

After the functional test, the simulated "brain" test was run. Since the saline-soaked simulated "brain" is placed into the well of the 64-pin package, a plastic sheet was placed over the package and elite board with a small square hole cut over the well. To seal the plastic onto the package, COAX-SEAL, a moldable plastic (Universal Electronics, Inc), was placed on both sides of the sheet around the cut.

For the unencapsulated brain chip test, a video camera was set up to record the eight traces of the oscilloscope. It was felt that the chip would fail quickly since sodium ions were to be placed directly on the unprotected array. The oscilloscope was configured to monitor the three least significant outputs of the counter (TS0 - TS2), one OUTPUT column, ROW#3, ROW#6, the input to the simulated "brain," and the

output of the simulated "brain". The count selected was for rows 1 - 8.

The simulated "brain" was then placed onto the electrodes. Within 0.25 seconds, the chip failed completely. It appeared that all traces immediately began displaying the simulated "brain" signal and this continued throughout the rest of the test. However, later observation of the recorded video in slow motion showed a definite pattern of failure. As the "brain" was placed onto the electrodes, the "brain" signal appeared immediately on the OUTPUT trace, with all other traces unchanged. Approximately 51 milliseconds later, the ROW signals began to break up and display the "brain" signal also. After approximately 255 milliseconds, the counter outputs also failed and displayed the "brain" signal.

This test showed the NMOS could read and output signals through the electrode array. However, it demonstrated how quickly sodium ions can destroy the electrical workings of an NMOS circuit. The final effect on the array was to permanently short the transistors formed by the electrodes, ROWs, and OUTPUT columns. Therefore, it is imperative the encapsulation process protect each of the 256 electrode array transistors.

Encapsulated Array Testing. The unencapsulated array test showed the importance of protecting the array. Therefore, a brain chip was encapsulated, packaged, and tested. The encapsulation was accomplished using the schedule developed in Chapter III. Bonding of the encapsulated chip was similar to the unencapsulated chip, except that the number of wires bonded was minimized. The bonding diagram appears in Appendix C.

The test set-up and the encapsulated chip packaging were identical to that of the unencapsulated chip testing. Functional testing, without the simulated "brain", was again accomplished, and the chip proved to be fully operational.

For the saline test, the oscilloscope was set up to monitor the least significant bit of the counter (TS0), the "brain" chip signal, the ROW#1 pulse, and OUTPUTs #1, #2, #8, #15, and #16. Using the ROW#1 pulse and the counter output, the location for any other row on the OUTPUT trace can be determined. The simulated "brain" signal was input directly into some of the electrodes to compare differences in bonded and unbonded electrode signal pick-up. The simulated "brain" was set up, without the saline solution, in the well of the package. Using an eyedropper, the saline solution was added onto the tissue, and signals immediately appeared on the oscilloscope.

The simulated "brain" signal was set to 8 millivolts peak-to-peak at 5 KHz. The chip operated normally, except that only the bonded electrodes were picking up the signals from the "brain". The level of the output signal from these electrodes was also 8 millivolts peak-to-peak. A changing bias was present on all "brain" signals, going from -20 millivolts below the trace when the saline was first added to the tissue, to over 100 millivolts above the trace (off the oscilloscope) by the end of the test. The bias stabilized often at +40 millivolts.

Although signals appeared on the electrodes bonded to pins, no signals appeared on any other electrodes. It was determined that the simulated "brain" was not really in contact with the electrodes. This easily occurs because the wires attached to the tissue force the simulated "brain" up out of the well. Therefore, the tissue was pressed

into the well. As the "brain" was pressed into contact with the chip, signals began to appear at other locations on the trace. These were from the electrodes contacting the simulated "brain", and they measured from 1 to 4 millivolts peak-to-peak. The DC bias on these signals varied with the bonded electrodes. This bias increased to approximately 100 millivolts as the "brain" was pressed against the chip, and decreased to zero millivolts as it was released. The peak-to-peak signal strength of the unbonded electrodes increased and decreased similarly.

The signals continued in a varying pattern for 26 seconds after pressing the tissue into contact with the chip. During this time, the counter trace and ROW trace functioned normally. After 26 seconds, though, the chip failed, and all traces displayed varying levels of the "brain" signal. The electrode transistors did not appear to short as the unencapsulated array electrodes had since the peak-to-peak levels were different for the various OUTPUTs displayed. Some resistance was present between the electrodes and the OUTPUT pads. It was not obvious at that time why the polyimide had not protected the chip longer.

Under microscopic observation, the reason for chip failure became evident. When the bond wires on the chip had been coated with polyimide, a small area over the counter (top left corner of Figure 1) had inadvertently been left uncoated. It appears the sodium ions were able to attack the circuit through this opening. This did not begin until the tissue was forced onto the chip. Chip failure was noted by loss of triggering on the oscilloscope, which results in loss of trace displays. Triggering for the scope came from the SYO pulse, which is a product of the counter circuit. Up to loss of the traces, the OUTPUT

signals appeared normal. This was verified by observing the test in slow motion from a video recording. Therefore, chip failure was initiated in the control circuitry and not in the electrode array (as in the case of the unencapsulated chip). It appears the polyimide did protect the electrode array throughout the test.

In an attempt to prove the conclusions from the test, it was repeated on a second encapsulated chip in a 64-pin package. This chip was prepared and wired identically to the first encapsulated test package. The functional test showed the chip was operational, but the outputs of the multiplexer (ROW pulses) were not well-defined pulses. The trailing-edge of each pulses was square, but the leading-edges contained some noise. The OUTPUT from the bonded electrodes appeared only when the noise stopped on each ROW pulse. It was felt that this noise would have no effect on the test.

When the saline was dropped onto the tissue to form the simulated "brain" on the chip, signals appeared immediately on the OUTPUT columns containing bonded electrodes. However, no unbonded electrode OUTPUTs were seen, except on OUTPUT#14. The "brain" signal was visible on the trace, but appeared very low in voltage level. After 10 seconds of operation, the decision was made to force the simulated "brain" against the chip, as in the previous test. When pressure was added, the chip failed immediately. The oscilloscope display went blank as the SYO trigger was lost. When the display was returned, all traces were blank except for the "brain" signal input. The electrode transistors were off, passing no signals through.

The failure of this chip occurred while applying force to the chip. It is possible that either the GND or VDD lead wire, beneath the epoxy

and polyimide, was broken due to the force. As mentioned in Chapter III, the epoxy is weakened after the high polyimide cure. Some bubbling occurs in the epoxy during this cure, also, and may lead to a hidden bubble below the surface. Externally, there does not appear to be any damage.

Although the chip's control circuitry was no longer operative, the transistors associated with the electrodes could still be used. The ROW lead wires were still attached to the chip and package, as were the OUTPUT leads. The electrode passes a signal through to the OUTPUT pad when the ROW pulse is high for that electrode. Therefore, with the simulated "brain" operating in the well of the package, +5 volts was applied to the ROW#1 pin of the package. Immediately, the "brain" signals appeared on the oscilloscope OUTPUT traces. When ROW#1 pin was grounded, the signals were no longer present. By attaching the elite board clock to the pin, the "brain" signal was switching off and on with the clock. Similar results were obtained with the other ROW pulses.

The electrode transistors operated normally throughout the rest of the test. The 8 millivolt "brain" signal was measured at 7 millivolts through the OUTPUTs. After 10 minutes, the test was terminated since there were no additional changes noted. This proved the polyimide encapsulation process was able to provide the needed protection for the electrode array. The only problem existing was in the epoxy/polyimide layers during packaging. Unfortunately, these problems were not identified until after the first implantable package was fabricated. Therefore, these same problems were to be repeated in final package testing.

Package Testing

With some success apparent in the circuit testing, the final implantable package was fabricated for testing. This testing was to be similar to the circuit testing, except it was to be long-term testing. The polyimide had proven its ability to protect the brain chip array in the simulated "brain," but no attempt had been made to determine how long this protection would hold. Since this was the type of package which would be implanted, this was the one which should undergo the long-term testing.

The test set-up was slightly different for final package testing. Since the implantable package has a connector on one end, the mating receptacle was wired into its own bread board strip, instead of the elite board. Power, ground, and clock connections were made to the elite board however. The other difference was in the placement of the simulated "brain". Since no well exists on this package, the simulated "brain" cannot be placed onto the chip. Instead, the simulated "brain" was permanently set up in a petri dish. The package could then be turned over and placed directly on the simulated "brain". This arrangement would also insure good contact between the simulated "brain" and the electrode array, without applying any external force.

Unfortunately, this package was completely inoperative, and could not be tested. It was during fabrication of this package that the inability of the epoxy to withstand the 180° C polyimide cure was discovered.

After bonding the lead wires from the chip to the kynor wires in the cylinder, the chip was functionally tested. Operation, although not perfect, was adequate for testing. The most significant bit of the

counter output (TS3) was not produced correctly, and the count pulses could not be varied correctly by the count select lines. The electrodes could not be tested since none were bonded. However, noise from the overhead fluorescent lights did appear on the OUTPUT lines as the multiplexer turned on each of the sixteen ROWs. Therefore, the chip appeared to be testable.

However, after application and cure of both the epoxy and polyimide (as described in Chapter III), the chip was completely inoperative. No control circuitry worked, and none of the three ROWs could be turned on manually. Due to some deformation of the epoxy, it was felt that some wires had broken. This would occur with this package much easier than with the 64-pin package, because wire bonds on the kynor wire were much more fragile than those to the gold-plated pads of the 64-pin package. If the epoxy softened then shifted during the polyimide cure, these wires would easily separate from the kynor wire.

A simple test was done on a 64-pin package to prove this. Eight different pins were bonded to the L-bar of an old, discarded brain chip. When tested for continuity with an ohm meter, all eight pins showed zero resistance to each other. After applying epoxy and curing it, seven of the pins still showed continuity. This suggests possible shrinkage of the epoxy, although the specification sheet for the epoxy did not mention any shrinkage. After applying the polyimide then curing for two hours at 180° C, only three pins showed continuity. Although no wires appeared damaged externally, four had separated from either the pins or the chip bonding pads. Prior 64-pin packages had appeared to contain broken wires, but these breakages had been assumed to be caused accidentally while applying epoxy by hand.

Despite the inability of the epoxy to protect the wires, another implantable package was fabricated. This package included redundant bonding for both VDD and ROW#9. It was felt that if just one row pulse could survive, the package could still be tested. To minimize polyimide shrinkage, the cure times at the lower temperatures were tripled. This all proved futile, as all wires again broke.

Since time did not permit identifying and acquiring of a high temperature epoxy, no further implantable packages were made. However, the long-term testing was still done. Using the encapsulated 64-pin package tested previously in the circuit test, and the alternative test set-up described at the beginning of this chapter, a long-term test was designed. The ROW pins of the 64-pin package had allowed the turning on and off of the electrodes in the array. Therefore, four functioning ROW pins were soldered to wire leads: ROW#5, ROW#8, ROW#14, and ROW#16. Three OUTPUT pins were also soldered to wire leads: OUTPUT#2, OUTPUT#8, and OUTPUT#16. The pins were soldered instead of inserted into an elite board to allow the package to be placed onto the simulated "brain" as the implantable package would have been.

The ROW leads were attached to the external control circuitry of the alternate test set-up. The ROWs could then count as originally designed. A large plastic sheet was placed on the 64-pin package as before, and sealed with COAX-SEAL to prevent the saline solution from corroding any of the package's pins. The package was then inverted, and placed onto the simulated "brain". The OUTPUT "brain" signals appeared on the traces only when the ROW pulses were on, as expected. With a 26 millivolt input signal from the Wavetek, the simulated "brain" produced a 9 millivolt sine wave. The electrode OUTPUTs varied

from a high of 8 millivolts when ROW#8 was on, to a low of 1 millivolt when ROW#16 was on. These variations are due to the contact of the chip and the "brain."

As in prior tests, a DC bias was present. However, while varying the input voltage to the ROWs, the bias changed. With the input voltage set at 0 volts, there are no signals at the OUTPUTs, and there is no bias on the "brain" signal. As the voltage is increased to +5 volts, the OUTPUTs begin registering the sine wave signal. The "brain" signal shows a slight positive bias, estimated to be less than 1 millivolt. As the voltage is increased to +5 volts, the "brain" signal as well as the OUTPUT signals shift up between +1 and +2 millivolts. Measurements below 4 millivolts could only be estimated on the oscilloscope used. This had not been noticed on any previous tests because the input voltage had never been varied during the short amount of time of those tests.

Since the chip being used was not a completely functional chip, it was not possible to precisely determine why the ROW inputs caused the DC bias shift in the "brain" signal. There are, however, two possible explanations: an ungrounded chip or leakage through the gate to source.

The chip under test was the second package tested in the encapsulated 64-pin package testing. Its control circuitry probably failed due to broken wires. Resistance checks with an ohm meter showed a 90 megohm resistance between the GND pin and the VDD pin and an 11.5 megohm resistance between GND and a multiplexer output (ROW#8). Therefore, it was suspected the GND wire had broken, making it impossible to ground the chip. This floating ground could have caused a capacitive

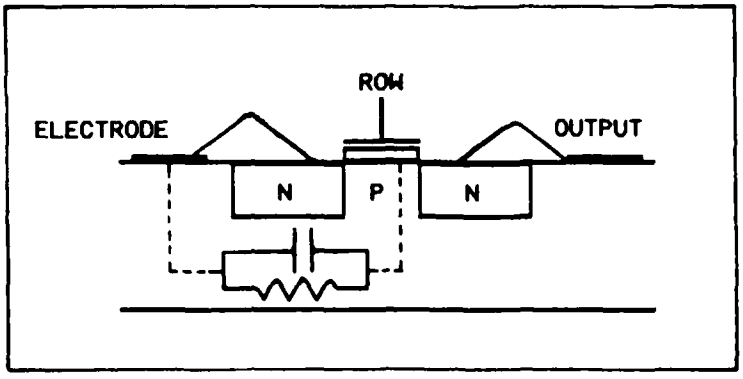

Figure 16. Capacitive Coupling Between NMOS Gate and Electrode Pad

coupling between the polysilicon gate and the electrode pad, as shown in Figure 16. This coupling can inject the DC from the gate into the brain, as well as into the electrode's associated transistor source. This would result in the DC bias, as observed.

It is also possible for the gate's DC to leak through the gate to the source. This leakage would also raise the "brain's" DC bias. Since the bias was very small (1 to 2 millivolts) compared to the input voltage (5 volts), this leakage could have occurred.

In either case, this problem must be researched further. There is a very serious consequence of this problem due to the injection of current into the brain. The validity of the readings from the brain chip may be questioned since they may partially result from the electrical stimulation of the ROW pulses instead of just visual stimulation.

Despite its possible electrical problems, the brain chip did continue to function normally for 21 days. There was only a slight loss of "brain" signal amplitude picked up by the electrodes. The test was terminated at this point, with the chip still functioning, to check for

any damage to the polyimide or aluminum electrodes. The chip was studied under a scanning electron microscope. There was no damage to the polyimide, as all the electrode openings were exactly as originally etched. However, the aluminum electrode pads did receive some damage. About 85 of the 256 pads received minor deterioration, while another 16 lost about one-third of the aluminum from the exposed pad. No aluminum beneath the polyimide was affected. All of the electrode damage was on electrode pads in columns 5, 8, and 16 - the only ones monitored for the full 21 days. This deterioration was probably responsible for the slight loss in signal.

Materials Testing

Prior to the long term package testing, the effects of a saline environment on polyimide and aluminum was tested. An encapsulated 64-pin package, similar to those tested above, was placed into a 0.9% NaCl solution. No voltage was applied to either the solution or the package. After two weeks, the package was removed. The only noticeable effects were corrosion of the package's pins. The aluminum electrodes and polyimide appeared intact. Observation under a scanning electron microscope revealed the polyimide layer around two different electrodes was damaged, but the damage did not appear to be a result of the saline environment. It appeared the layer may have been scratched causing a portion of the layer to break off. The aluminum electrodes showed no effects from the saline solution.

Analysis

The NMOS circuit will pick up and transmit the signals as well as the 4 X 4 JFET array did. There is little loss in pick-up of signals

through the aluminum electrodes at the frequency used (5 KHz). However, the circuit is extremely vulnerable to sodium contamination when unprotected. The circuit could not operate for even one second in a saline environment.

Polyimide will protect the electrode array in the corrosive environment, though. This protection has been proven to hold up for 21 days of continuous brain chip operation. However, if no current is passing through the exposed pads, as in the Materials Testing section above, the pads show little, if any, deterioration.

In vitro operation of the chip's control circuitry for long periods of time could not be shown. The failures do not seem to point to the inability of the polyimide to protect, but rather to the epoxy's ability to protect the wires. In one case, a hole was left unprotected over the chip's counter. However, in the other test cases, the wires either did not survive polyimide curing or broke when pressure was applied. One test did prove that polyimide curing can break wire bonds despite the epoxy layer, but actual proof of this is impossible to detect through the epoxy layer. However, if an epoxy capable of withstanding 180° C for two hours can be found, the above tests should prove the polyimide process and implantable package fabrication valid.

The only unanswered problem is the DC bias injected into the brain by the ROW gates. Since there is always one ROW high during chip operation, the overall effect will be a constant DC voltage applied to the brain. This DC bias would be approximately 1 to 2 millivolts, compared to actual brain signals up to several hundred microvolts (4:88). It is unclear what effect this will have on the recorded brain signals, since it is possible this bias could stimulate the brain. This problem may

only be caused by a floating ground, and may not appear in a completely functional chip. However, the problem may be peculiar to the NMOS circuitry, and exist in functional chips also. Further testing must be accomplished in vitro with a completely functional, encapsulated array.

V. Problems and Techniques

During development of the encapsulation processing schedule, a number of problems were encountered which necessitated modification of procedures or equipment prior to continuation. These problems were the result of using individual integrated circuits for processing instead of larger wafers. The equipment used in processing is designed for wafers ranging from one to three inches in diameter. The NMOS brain chip used in this work measured 9/32 inches on a side. The brain chip with multiplexed outputs will be even smaller due to the decrease in the number of output pads. Since NMOS chips supplied by MOSIS are returned pre-cut, any continuation work in this area at AFIT will require use of the same equipment. Therefore, this chapter is included to detail modifications and techniques that will aid in processing.

Equipment Modifications

The equipment in which problems exist are: the spinner and the mask aligner. In both cases, the brain chip is too small to create a vacuum on the chuck on which it sits. This is due to the spread of the holes around the chuck - the chip simply cannot cover all the holes. Without the vacuum, processing on the equipment is impossible. With the spinner, lack of a vacuum results in the chip flying off the spinner when it is started. In the case of the mask aligner, the chip does not move consistently with the chuck when under the mask, making alignment impossible. Both problems were solved using different modifications.

Spinner. To solve the spinner problem, the vacuum holes on the

chuck were sealed, except for the center hole. This was done on the smallest chuck available - a 1-inch diameter chuck. The sealant used was RTV silicone sealant (Dow Chemical). It was spread evenly across the entire top surface of the chuck, leaving only the center hole uncovered. The surface must be smooth to allow the chip to lie flat and optimize the vacuum of the spinner. The RTV must be allowed to cure 24 hours prior to use.

The results using this modified chuck were excellent for application of polyimide and photoresist. However, due to the small size of the chip, these chemicals will also be deposited onto the RTV surface of the chuck. Since the chip may not seal completely on the chuck, some of these chemicals will be sucked down the vacuum through the hole in the center (beneath the chip). Although this will not affect the chip, it will decrease the vacuum, and possibly seal the center hole if allowed to accumulate. The chuck and vacuum line should, therefore, be cleaned with small amounts of AZ351 and acetone periodically to prevent loss of vacuum.

Although this chuck worked well with polyimide and photoresist, it did not work well with the negative photoresist developer chemicals. Both the Xylene and Butyl Acetate quickly attacked the RTV while spinning on these chemicals. Continued use will strip the RTV resulting in loss of vacuum. Therefore, an additional modification was required. By attaching a small square of double-sided tape to the center of a 1-1/2 inch diameter wafer, the chip could be held in place while spinning. The tape should be small enough to fit completely beneath the chip to prevent the chemicals from attacking the tape. The tape should be centered to minimize the centrifugal forces on the spinning chip.

The tape on the wafer allows full-speed operation of the spinner. It could also be used with the polyimide and photoresist, except for two disadvantages. The primary disadvantage is the sticky residue which adheres to the back of the chip when it is removed from the tape. If not removed, it will bake onto the back resulting in an uneven surface. Both developing and etching can be accomplished without removing the chip from the tape. Therefore, the tape residue can be removed with an X-ACTO knife after etching, then put into the oven for cure. If this wafer were used for both polyimide and photoresist also, the residue would have to be removed after each was applied. The other disadvantage is that the tape must be replaced after the chip is removed. If the tape is used for another chip, it may not retain enough adhesion material to hold a fast spinning chip.

By using the modified chuck for polyimide and photoresist, and the modified wafer for developing and etching all spinner problems were overcome.

Mask Aligner. The modification for the mask aligner vacuum problem was solved using a large wafer to hold the chip. The mask aligner requires 3-inch wafers to obtain the vacuum. Tape could not be added to the center of a 3-inch wafer, though, as this would have made the chip sit too high above the chuck. With the chip too high, it would remain in contact with the mask when it should be separated for aligning. Therefore, a wafer had to be cut to hold the chip.

The modification required cutting a 3/8-inch strip from the center of a 3-inch wafer. A 1-1/4 inch long strip was then cut and discarded from the center of this strip, resulting in four pieces of wafer. These pieces should then be reassembled into a 3-inch wafer on a sheet

of paper coated with rubber cement. The final result is a 3-inch wafer with a 3/8 by 1-1/4 inch strip of paper exposed in its center. The exposed paper will still have some rubber cement which, when dry, will help to hold the chip in place.

This modified wafer will hold the vacuum on the chuck and the cut-out strip will hold the chip. The strip is much larger than the chip so the chip can be moved, as needed, to aid in the alignment. In some locations on the wafer, the chip will not be within reach of a mask pattern while in the alignment position. It will, therefore, be necessary to relocate the chip in the cut-out portion of the wafer. Using this modified wafer, alignment of individual chips became possible.

Processing Techniques

Not only must processing equipment be modified, but new processing techniques must be used when working with individual chips. The size of the chips makes handling difficult and requires a great deal of attention to detail. Processing of an individual chip can be aggravating, but these techniques can aid in a better yield.

When handling chips, it is best to use a set of nonmetallic tweezers. The small size of the chips makes them difficult to pick up and carry. It is very easy to scratch the surface when trying to grasp with tweezers. Stainless steel tweezers will often scratch through the surface and destroy metal runs below the passivation layer. A set of plastic or Teflon tweezers is best.

As mentioned in Chapter III, a meniscus builds up on the edge of the chip during processing. It is very important that the surface tension is broken prior to spinning, to minimize this meniscus.

Therefore, when applying adhesion promoter, polyimide, and photoresist, allow it to coat the surface as well as the sides of the chip.

The brain chips are very light compared to silicon wafers. Shots of N_2 must be applied very carefully, or the chip will fly out of the tweezers. Care must also be taken when using a convection oven. If the fan is too strong, it will blow the chips around in the oven. This is especially true when opening and closing the oven door. The fan must be turned off prior to opening the door.

Since wire baskets are too large to hold chips in the oven, small wafers can be used. The 1-1/2 inch wafers were ideal for this purpose. However, when spinning polyimide or photoresist onto the chip, some residue may accumulate on the bottom surface. When baked, this residue will dry causing the chip to stick to the wafer. An X-ACTO knife or razor blade should be used to help separate the chip. If too much pressure is applied, the chip will break. As a last resort, the wafer and chip should be soaked in acetone to free the chip.

Use of these techniques increases the processing yield, since they minimize damage to chips. However, the most important technique is attention to detail - do all processing deliberately, and patiently.

VI. Conclusions and Recommendations

Conclusions

Polyimide has proven successful in protecting a JFET integrated circuit in an actual cerebro-spinal fluid (CSF) environment in prior work. Using a new circuit and new processing schedule, it was shown to protect an NMOS integrated circuit in a simulated CSF environment. A new package, designed for chronic implantation, appears viable.

New Circuit. The new NMOS brain chip includes a 16 X 16 array of aluminum electrodes output through 16 output pads. It has been tested both in and out of a saline environment. Without any protective layer (other than its standard glass coating), the circuit will work in a simulated CSF for less than 1 second. The sodium ions cause permanent catastrophic failure, almost immediately. However, the circuit does read signals through the electrodes, and sends them to the output pads.

With a polyimide coating of 8 microns, the circuit will work for a minimum of 3 weeks, with no damage to the protected circuitry. However, the exposed aluminum pads will deteriorate in the saline solution, while current is passing through them. The pads will transfer input signals for about 3 weeks of continuous use with little signal loss. However, as the pads deteriorate, the signal loss increases. When there is no current passing through the pads, their deterioration is greatly reduced.

There is, however, the possibility the NMOS brain chip may inject a constant DC bias into the brain while in operation. The source of the DC is the output of the multiplexer (ROW pulses). Measured at 1 to 2 millivolts, this DC may have occurred only because the circuit under

test could not be grounded. However, it is possible that this DC may be leaking from the gate to the source. The effects of this constant DC on the brain are not completely known, but may affect the validity of brain signal readings. Therefore, further in vitro testing with a completely functional chip is essential.

Processing Schedule. Basing a processing schedule on the negative photolithography process used by Hensley and Denton, a new encapsulation process was developed. Although a number problems were encountered processing individual chips (versus a wafer), modifications in equipment and processing techniques resolved these problems. The most important breakthrough was in minimizing the meniscus build-up on the edge of the chip, by breaking the meniscus prior to spinning on the polyimide or photoresist. Until this was discovered, there was no success in etching a satisfactory pattern on an individual chip.

Using processing Schedule #4 in Appendix A, an 8 micron thick layer of polyimide was added to the surface of the chip. This protective layer definitely protected the electrode array from the simulated CSF environment, allowing up to 15 days of continuous operation in it. According to the literature reviewed during this effort, polyimide will absorb moisture, and begin losing its excellent electrical properties. Polyimide, therefore, is not the best encapsulant, but appears to provide more than adequate protection for its intended use, as shown in the testing.

However, there were problems associated in each test which resulted in loss of the control circuitry of the chip. These problems were usually due to inadvertent oversights in packaging, in addition to a serious packaging problem.

Brain Chip Packaging. Packaging of the brain chip involves not only hooking the chip to the outside world, but protecting the hook-up and chip from both physical and electrical damage. The package designed in this thesis does allow for communication to the outside world through a small cylindrical package. The package, with an encapsulated brain chip on one end and a 85-pin connector on the other, fits into a larger cylindrical mount designed to be permanently mounted in the skull of a rhesus monkey. The package is easily inserted and removed from the test subject, and can be interchanged with other like units. The connector attached to one end of the package allows the package to remain in the skull without having to be physically wired to any recording device: this connection is made only for actual tests with the monkey. The advantage of the design is the easy access to the implantable device, without chronic surgery. The only surgery required is in affixing the cylindrical mount permanently in the skull. A surgical procedure using a similarly shaped device has already been developed by the Aerospace Medical Research Laboratory and can easily be adapted for use with this package.

However, a serious problem arose which prevented successful completion of an actual package. The epoxy used to hold the chip, the hook-up wires, and fragile chip bond wires failed. The high heat required to thoroughly cure polyimide softens the hardened epoxy, allowing the bond wires to break. Both packages fabricated were completely useless, as most of the wires to the chip broke. This problem was not solved due to lack of time.

Recommendations

Additional effort is needed to bring about implantation. This work must be done in the area of packaging. This thesis effort suggests new areas of research in packaging, processing, and testing.

Packaging. One of the most important areas requiring additional effort is the packaging of the brain chip. Especially important is the selection of a different epoxy. The epoxy used, Epotek H70E, does not hold its rigidity during the final cure of the polyimide. The epoxy must protect the fragile bond wires during this critical curing stage. Therefore, it is imperative a new epoxy be found. This new epoxy must have an operating temperature of at least 180° C, since it will be at this temperature for two hours. The epoxy must, of course, be an electrically insulating epoxy. Packaging cannot be completed until this new epoxy is found.

The type of hook-up wire used in packaging should be replaced. The present type, a solid, copper wire insulated by kynor is guaranteed to 125° C, according to a number of electrical supply catalogs. It has been used successfully, though, at 180° C. Although no wires have shorted together, the insulation after high temperature cures has shown signs of fatigue. If possible, Teflon coated wires should be used. The only requirement is the wire must be solid, not stranded.

Due to availability, the connector used in packaging was an 85-pin microminiature connector, by ITT Cannon Electric. This was the only company found which manufactures such small connectors with a high pin-out. Only 35 of the 85 pins were required. Although a 35-pin connector would be ideal, the next smallest connector with at least 35 pins is a 55-pin connector by Cannon. This connector has been ordered for

further research. However, if an equally small connector, with a minimum of 35-pins can be found, it should be used.

To insulate the solder connections between the kynor hook-up wires and connector wires, RTV sealant is suggested. If available in a 30-gauge size, heat-shrink tubing could also be used to provide this insulation. This will allow the maximum room possible for pushing wires back into the cylinder when attaching the connector to the top.

Processing. The biggest recommendation for the processing phase is to use wafers instead of individual chips. In addition to requiring no equipment modification, it relieves a great deal of aggravation which results from working with small chips. Each individual chip requires the same amount of processing time as a whole wafer. Therefore, using a wafer will save an enormous number of man-hours in processing. The only additional processing step would then be to cut the chips from the wafer. However, the equipment and expertise exists at Wright-Patterson AFB to accomplish this.

Testing. Testing in this thesis left open a possible problem of an NMOS brain chip. Since it is not known whether a functional brain chip will inject unwanted voltages into the brain, it is recommended that additional in vitro testing be accomplished prior to use. This testing should include testing of encapsulated chips with silver electrodes to determine if there is less deterioration than with aluminum.

Further Research. Further research efforts should initially be toward implantation of this package. It must be shown whether the chronic implant is a feasible process with no adverse effects to the monkey. Using this type of implant will allow any type of circuit to be used, as long as it will fit on the implantable cylinder.

Additional research effort must be directed toward correcting the problem with the multiplexed output chip. The multiplexed output brain chip will minimize the number of connections to the chip by at least eighteen wires. It may then be possible to go to a smaller connector since Cannon also carries a 19-pin microminiature connector. This chip has already been tested, and the results recorded (Appendix F). These results only need to be studied to determine the reason for failure, then the file corrected. If the multiplexed output chip is used, it may be possible to redesign a smaller package.

If a smaller package can be designed, the full capabilities of the brain chip can then be realized: interconnection of two brain chips. This interconnectability was designed into the brain chip through the SYO and SYI pads. The chip remains dormant until its SYI input transitions to low. The chip then goes through its count (depending on the count select inputs). When its count is finished, the chip's SYO transitions to low, reviving the other chip, and goes back to its dormant state. Interconnection also allows one chip to be used to input, while the second records output. In this way, pictures can be input to the primary visual cortex, and results of this input sensed at the secondary visual cortex. Although this is possible with the present design, it will require removal of a large area of the skull, leaving the monkey vulnerable to injury. Therefore, this area of research should be preceded by a redesign of the package.

Appendix A

Photolithography Processing Schedules

Standard Clean

This is the standard cleaning schedule used prior to processing any wafers or chips. This cleaning eliminates organic contaminats from the surface. The one hour bake out is a minimum time and removes all moisture from the chip.

1. Dip in beaker of acetone - removes organic material.
2. Blow dry with N_2.
3. Flood with methanol - removes more organic material.
4. Blow dry with N_2.
5. Flood with de-ionized water (DIW).
6. Blow dry with N_2.
7. Bakeout one hour (minimum)in convection oven at 220° C, N_2 ambient - removes moisture from surface.

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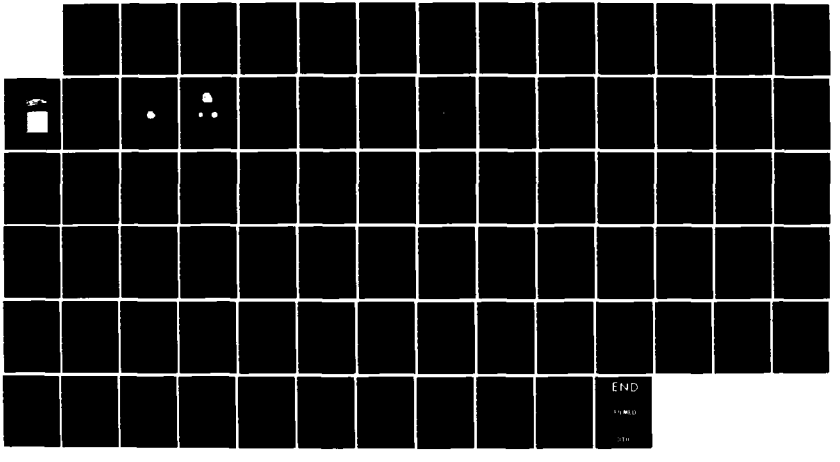
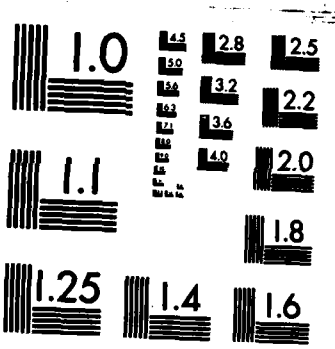




Schedule #1: Positive PR Process for Wafers

This process was used to establish a consistent photolithography process for using AZ1350J positive photoresist.

1. Clean using Standard Clean process and 220° C oven.
2. Preheat second oven to 70° C.
3. Remove wafer from 220° C oven after bakeout and allow to cool.
4. Blow clean with N_2.
5. Apply adhesion promoter (HMDS):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 3 krpm for 30 sec - dries HMDS.
6. Apply positive photoresist (AZ1350J):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 3 krpm for 30 sec.
7. Prebake photoresist - 70° C for 20 minutes.
8. Blow clean with N_2.
9. Align/expose - 20 seconds.
10. Develop photoresist:
    - puddle AZ351 developer (1:5 with DIW).
    - spin/spray @ 1 krpm for 15 sec (spray only enough to keep wet).
    - puddle DIW (to rinse and stop developer).
    - spin/spray @ 2 krpm for 30 sec.
    - spin/dry @ 5 krpm for 30 sec.
11. Examine pattern under microscope - look for fully developed pattern across wafer; if any over-developed patterns or undercutting, decrease AZ351 develop time or exposure time.
12. If not fully developed repeat step 10.

Schedule #2: Polyimide/Positive PR Process for Wafers

The following schedule was used to establish a consistent photolithography process using polyimide and positive photoresist on practice wafers. However, no consistent process could be found. The schedule below was the basis for the numerous attempts at finding a successful schedule.

The primary variables changed were the develop times, the postbake temperature, the etch times, and the etchant used. This schedule does not produce acceptable results.

1. Clean wafers using Standard Clean process and 220° C oven.
2. Preheat second oven to 70° C.
3. Remove wafer from 220° C oven after bakeout and allow to cool.
4. Blow clean with N_2 - removes surface dust.
5. Apply polyimide adhesion promoter (VM-651):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 10 sec.
   - spin @ 5 krpm for 30 sec.
6. Apply polyimide (PI 2555):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 6.5 krpm for 30 sec.
7. Prebake PI 2555 at 70° C for 20 minutes, N_2 ambient - dries the polyimide without curing; place in oven immediately to minimize formation of pinholes.
8. Remove from oven, and allow to cool.
9. Blow with N_2 - removes surface dust.
10. Apply adhesion promoter (HMDS):
    - puddle on wafer.
    - spin/spread @ 2 krpm for 5 sec.
    - spin @ 3 krpm for 30 sec - dries HMDS.

11. Apply positive photoresist (AZ1350J):
    - puddle on wafer.
    - spin/spread @ 2 krpm for 5 sec.
    - spin @ 5 krpm for 30 sec.

12. Prebake photoresist at 70° C for 20 minutes, N_2 ambient.

13. Blow clean with N_2.

14. Align/expose - 20 seconds.

15. Develop photoresist:
    - puddle AZ351 developer (1:5 with DIW).
    - spin/spray @ 1 krpm for 20 sec (spray only enough to keep wet).
    - puddle DIW (to rinse and stop developer).
    - spin/spray @ 2 krpm for 30 sec.
    - spin/dry @ 5 krpm for 30 sec.

16. Examine pattern to determine if additional developing required.

17. Postbake at 100° C for 20 minutes, N_2 ambient - toughens photoresist.

18. Etch the polyimide:
    - AZ351 (1:5) bath - 30 sec.
    - DIW bath - 30 sec.
    - Blow dry with N_2.

19. Examine - check for full etch without PR lifting or pattern breaking.

Schedule #3: Polyimide/Negative PR Process for Wafers

This schedule outlines a consistent photolithography process using polyimide and negative photoresist on 3-1/2 inch practice wafers. Prior to applying an additional coat, the polyimide must be fully cured.

1. Clean wafers using Standard Clean process and 220° C oven.
2. Preheat second oven to 70° C.
3. Remove wafer from 220° C oven after bakeout and allow to cool.
4. Blow clean with N_2 - removes surface dust.
5. Apply polyimide adhesion promoter (VM-651):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 10 sec.
   - spin @ 5 krpm for 30 sec.
6. Apply polyimide (PI 2555):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 6.5 krpm for 30 sec.
7. Prebake PI 2555 at 70° C for 20 minutes, N_2 ambient - dries the polyimide without curing; place in oven immediately to minimize formation of pinholes.
8. Remove from oven, and allow to cool.
9. Blow with N_2 - removes surface dust.
10. Apply negative photoresist (Waycoat Type 3, 28 CP):
    - puddle on wafer.
    - spin/spread @ 5 krpm for 30 sec.
11. Prebake photoresist at 70° C for 20 minutes, N_2 ambient.
12. Blow clean with N_2.
13. Align/expose - 4.5 seconds.
14. Develop photoresist:
    - spin/spray Xylene @ 1 krpm for 20 sec (spray enough to keep wet).
    - spin/spray Butyl Acetate @ 1 krpm for 20 sec.
    - spin/blow N_2 @ 1 krpm for 30 sec.

15. Examine pattern to determine if additional developing required.

16. Postbake at 120° C for 20 minutes, N_2 ambient - toughens photoresist.

17. Etch the polyimide:
    - AZ351 (1:5) bath - 5 sec.
    - DIW bath - 30 sec.
    - Blow dry with N_2.

18. Examine - check for full etch without PR lifting or pattern breaking; reaccomplish etch, if required.

19. Cure at 180° C for 2 hours, N_2 ambient - full cure prior to an additional coat.

Schedule #4: Polyimide/Negative PR Process for a Chip

This schedule outlines the photolithography process using polyimide and negative photoresist on a single brain chip. This schedule is consistent. Its differences from the wafer schedule resulted from differences in size of wafers and a single chip.

1. Clean chip using Standard Clean process and 220° C oven.
2. Preheat second oven to 70° C.
3. Remove chip from 220° C oven after bakeout and allow to cool.
4. Blow clean with N_2 - removes surface dust.
5. Apply polyimide adhesion promoter (VM-651):
   - puddle on chip, allowing it to spread onto chuck - coats the sides of chip.
   - allow to sit for 5 sec - insures good contact with side of chip.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 5 krpm for 30 sec.
6. Apply polyimide (PI 2555):
   - puddle on chip, allowing it to spread onto chuck - coats the sides of chip.
   - allow to sit for 5 sec - insures good contact with side of chip.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 6.5 krpm for 30 sec.
7. Prebake PI 2555 at 70° C for 20 minutes, N_2 ambient - dries the polyimide without curing; place in oven immediately to minimize formation of pinholes.
8. Remove from oven, and allow to cool.
9. Blow with N_2 - removes surface dust.
10. Apply negative photoresist (Waycoat Type 3, 28 CP):
    - puddle on chip, allowing it to spread onto chuck - coats the sides of chip.
    - allow to sit for 10 sec - insures good contact with side of chip.
    - spin/spread @ 5.5 krpm for 30 sec.
11. Prebake photoresist at 85° C for 20 minutes, N_2 ambient.

12. Blow clean with N_2.

13. Align/expose - 4.5 seconds (increase to 4.6 after 3 coats).

14. Develop photoresist:
    - spin/spray Xylene @ 1 krpm for 8 sec.
    - spin/spray Butyl Acetate @ 1 krpm for 10 sec.
    - spin/blow N_2 @ 1 krpm for 30 sec.

15. Examine pattern to determine if additional developing required.

16. Etch the polyimide:
    - spin/spray AZ351 (5:1) @ 1 krpm for 6 sec.
    - spin/spray DIW @ 1 krpm for 15 sec.
    - spin/blow with N_2 @ 4 krpm for 30 sec.

17. Examine - check for full etch without PR lifting or pattern breaking; reaccomplish etch, if required.

18. Cure at 150° C for 2 hours, N_2 ambient - partial cure of polyimide.

19. Remove photoresist - scrub lightly in acetone bath with a cotton swab; removes photoresist layer without harming polyimide layer.

20. Cure at 180° C for 2 hours, N_2 ambient - full cure of polyimide; required prior to additional coat of polyimide.

21. Repeat schedule for a minimum of 5 coats - start with step 4 if no break in processing, otherwise start with step 1.

Schedule #5: Positive PR Process for Chip Metallization

This process was used to expose the electrodes on the chip for metallization, using AZ1350J positive photoresist.

1. Clean using Standard Clean process and 220° C oven.
2. Preheat second oven to 70° C.
3. Remove wafer from 220° C oven after bakeout and allow to cool.
4. Blow clean with N_2.
5. Apply adhesion promoter (HMDS):
   - puddle on chip, allowing it to spread onto chuck - coats the sides of chip.
   - allow to sit for 5 sec - insures good contact with side of chip.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 4 krpm for 30 sec - dries HMDS.
6. Apply positive photoresist (AZ1350J):
   - puddle on chip, allowing it to spread onto chuck - coats the sides of chip.
   - allow to sit for 5 sec - insures good contact with side of chip.
   - spin/spread @ 4 krpm for 30 sec.
   - spin @ 4 krpm for 30 sec.
7. Prebake photoresist - 70° C for 20 minutes.
8. Blow clean with N_2.
9. Align/expose - 30 seconds.
10. Develop photoresist:
    - spin/spray AZ351 developer (1:5 with DIW) @ 1 krpm for 45 sec - spray hard occasionally to remove PR inside patterns.
    - spin/spray DIW @ 1 krpm for 30 sec - stops developer.
    - spin/blow N_2 @ 4 krpm for 30 sec.
11. Examine pattern under microscope - look for fully developed pattern in the array, since this is the only portion of the chip which will receive metal.
12. If not fully developed repeat step 10, as needed.

Appendix B

Materials Used and Manufacturers

Dupont: - Pyralin Polyimide, PI-2555
- Adhesion Promoter, VM-651
- Thinner, T-9035

E. I. Dupont de Nemours & Co. (Inc.)
Wilmington, DE 19898

Microposit: - Positive Photoresist, AZ1350J
- Positive Photoresist Developer, AZ351

Shipley Co., Inc.
Newton, MA

Waycoat: - Negative IC Resist, Type 3, 28 CP

Philip A. Hunt Chemical Corp.
Palisades Park, NJ 07650

SCM: - Positive Photoresist Adhesion Promoter, Hexamethyldisilizane (HMDS)

Organic Chemicals Division
SCM Corporation

Appendix C

Chip to Package Bonding Diagrams

Three bonding diagrams are included in this appendix, as well as the color codes for the implantable package wiring.

Bonding Diagrams

The first bonding diagram, shown in Figure 17, is for the unencapsulated chip in the 64-pin package used in the first test in Chapter IV. The second bonding diagram (Figure 18) is for the two encapsulated chips in 64-pin packages used in the second test. The last bonding diagram, Figure 19, is for the implantable package fabricated using the design in Chapter II and procedure in Chapter III. This figure shows the relationship of the chip's bonding pads to the wire tops of the package. The color coding and numbering of the wires as connected to the brain chip are shown in Table IV.

Implantable Package Wiring/Connector Coding

The connector used in this thesis was an 85-pin microminiature connector from ITT Canon Electric (see Appendix D). Only the 35 innermost wires were used to connect the chip to the connector. The coding of these connections is listed below, showing the wire number and predominant color/stripe as well as chip function (see Figures 1 and 19).

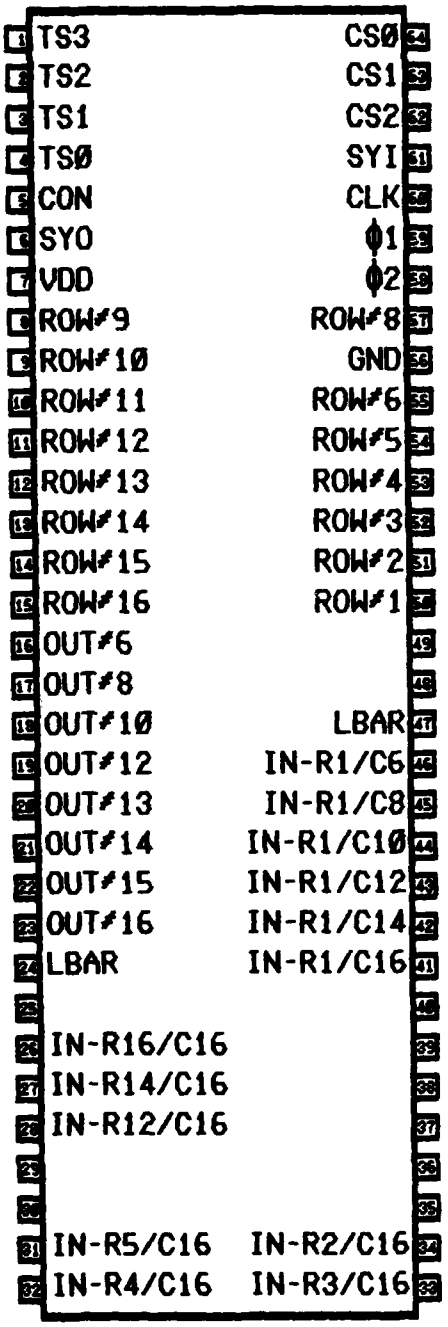


Figure 17. Bonding Diagram for an Unencapsulated Chip in a 64-Pin Package

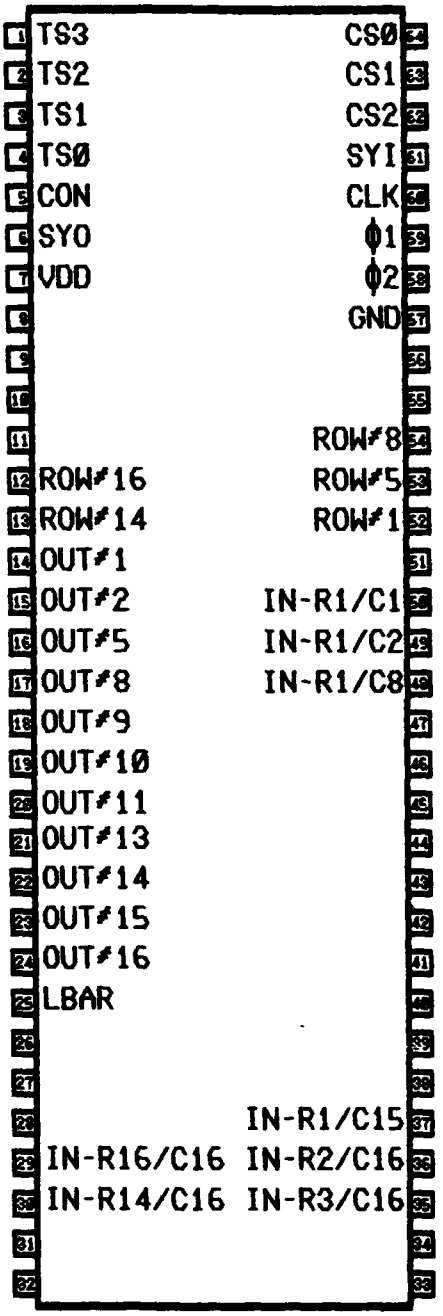


Figure 18. Bonding Diagram for an Encapsulated Chip in a 64-Pin Package

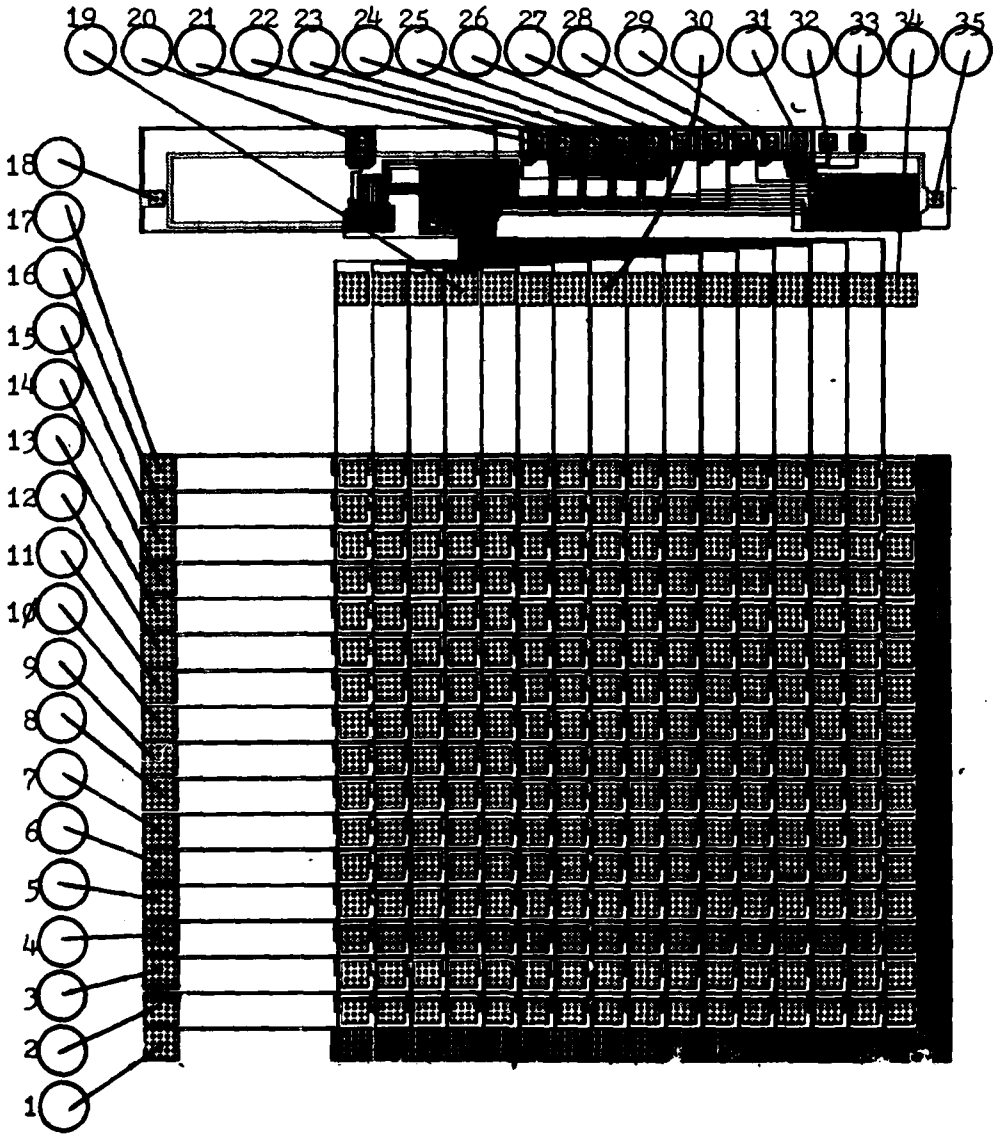


Figure 19. Bonding Diagram for an Encapsulated Chip in an Implantable Package

Table IV

Chip to Implantable Package Color Coding and Wire Numbering

CONNECTOR		BRAIN CHIP		
Wire #	Wire Color	Wire #	Wire Color	Function
14 -	White/Orange	1 -	Brown	LPAD
15 -	White/Yellow	2 -	Red	OUTPUT#16
16 -	Black	3 -	White	OUTPUT#15
17 -	Brown	4 -	Lt Blue	OUTPUT#14
22 -	Blue	5 -	Yellow	OUTPUT#13
23 -	Purple	6 -	Orange	OUTPUT#12
24 -	Gray	7 -	Dark Blue	OUTPUT#11
25 -	White/Lt Beige	8 -	Gray	OUTPUT#10
26 -	White/Black	9 -	Black	OUTPUT#9
31 -	Black	10 -	Brown	OUTPUT#8
32 -	Brown	11 -	Red	OUTPUT#7
33 -	Red	12 -	White	OUTPUT#6
34 -	Orange	13 -	Lt Blue	OUTPUT#5
35 -	Yellow	14 -	Yellow	OUTPUT#4
36 -	Green	15 -	Orange	OUTPUT#3
41 -	White/Black	16 -	Dark Blue	OUTPUT#2
42 -	White/Brown	17 -	Gray	OUTPUT#1
43 -	White/Red	18 -	Black	VDD
44 -	White/Orange	19 -	Brown	ROW#13
45 -	White/Yellow	20 -	Red	SYO
50 -	Yellow	21 -	White	CON
51 -	Green	22 -	Lt Blue	TS0
52 -	Blue	23 -	Yellow	TS1
53 -	Purple	24 -	Orange	TS2
54 -	Gray	25 -	Dark Blue	TS3
55 -	White/Lt Beige	26 -	Gray	CS0
60 -	White/Yellow	27 -	Black	CS1
61 -	Black	28 -	Brown	CS2
62 -	Brown	29 -	Red	SYI
63 -	Red	30 -	White	ROW#9
64 -	Orange	31 -	Lt Blue	CLK
69 -	Gray	32 -	Yellow	ϕ1
70 -	White/Lt Beige	33 -	Orange	ϕ2
71 -	White/Black	34 -	Dark Blue	ROW#1
72 -	White/Brown	35 -	Gray	GND

Appendix D

Specifications for the 85-Pin and 55-Pin Connectors

The connector used in this thesis was the ITT Cannon Electric 85-pin microminiature connector. It is composed of a plug (Figure 20) and receptacle (Figire 21), with the following stock numbers:

plug - MIKM6-5-85-PH054
receptacle - MIKM0-5-85-SH054

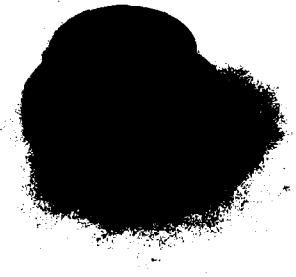


Figure 20. 85-Pin Microminiature Plug

The connector which should be used for further research is the 55-pin connector by ITT Cannon Electric, with the following stock numbers and prices:

plug - MIMK6-4-55-PH001 - $157.00 each
receptacle - MIKM0-4-55-SH001 - $186.00 each

The 85-pin connector was used for this thesis due only to its availability. The specifications for the 85-pin connector are very

Figure 21. 85-Pin Microminiature Receptacle

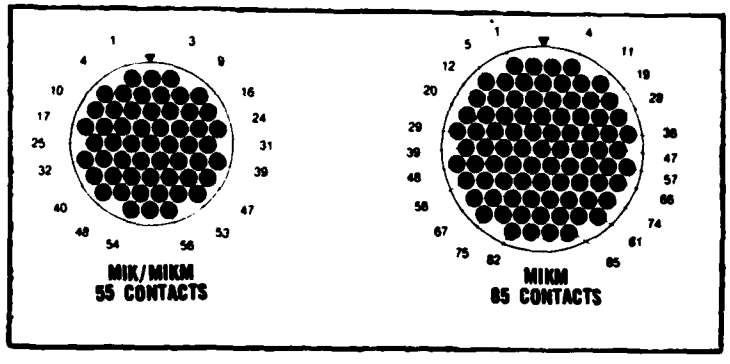
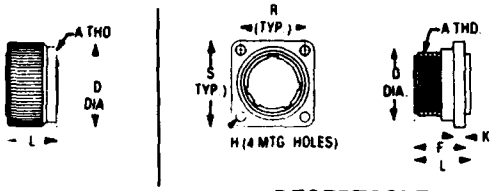


Figure 22. 55-Pin and 85-Pin Contact Arrangements

close to those for the 55-pin connector, as seen in Table V. The contact arrangement for both is shown in Figure 22.

Table V

Microminiature Connector Shell Dimensions



PLUG **RECEPTACLE**

Size 4

PLUG

Part Number by Shell Size	A Thread	B Max.	L Max.
MIKM68-1-7P	5/16-24UNEF-2B	.375(9.52)	.315(8.00)
MIKM68-4-8SP	5/8-24UNEF-2B	.755(19.18)	.440(11.18)
MIKM68-5-8SP	13/16-24UNEF-2B	.860(21.84)	.440(11.18)

RECEPTACLE

Part Number by Shell Size	A Thread	B	F Max.	M ±.003(±0.08)
MIKM0-1-7S	5/16-24UNEF-2A	.325(8.26)	.320(8.13)	.078(1.98)
MIKM0-4-8SS	5/8-24UNEF-2A	.625(15.88)	.426(10.82)	.091(2.31)
MIKM0-5-8SS	13/16-24UNEF-2A	.745(18.92)	.426(10.82)	.091(2.31)

Part Number by Shell Size	K	L Max.	R ±.005(±0.13)	S Max.	T Max.
MIKM0-1-7S	.062(1.57)	.400(10.16)	.460(11.68)	.630(16.00)	.032(0.81)
MIKM0-4-8SS	.062(1.57)	.490(12.45)	.580(14.73)	.760(19.30)	.125(3.18)
MIKM0-5-8SS	.062(1.57)	.490(12.45)	.674(17.12)	.845(21.46)	.125(3.18)

Appendix E

Report on Brain Chip Array with Count Selectable Multiplexer

This appendix contains a report written by Robert Ballentine as part of his course work for a VLSI design course at the Air Force Institute of Technology. The appendicies for the report have not been included as appendicies. The two computer programs, formerly Appendix A of the report, have been included at the end of the report. The computer generated plots, formerly Appendix B of the report, contain the same information found in Figures 1 and 2 of this thesis. The figures and tables in the report were renumbered to agree with the figure numbering of this thesis. The tables in the report appear at the end of the report, prior to the computer programs.

BRAIN CHIP ARRAY
with
COUNT SELECTABLE MULTIPLEXER

INTRODUCTION:

A brain chip array is designed to be implanted inside the skull of a living biological specimen, where the array electrodes contact the brain, detecting electrical signals. These signals are then transmitted by wire through the skull to an external recording device. Without any multiplexing, an individual wire would be required for each electrode. Thus, a 16 X 16 array would require 256 wires, which is an unmanageable number of wires and must be reduced. By multiplexing the sixteen rows to sixteen parallel column outputs, the number of wires is reduced to sixteen. Finally, by multiplexing the sixteen column outputs to a single serial output string, the number of wires can be reduced to one. This figure does not take into account the other wires required to input/output various signals, power, and ground. Future brain chip designs may eventually eliminate all wires; however, that issue will not be further addressed here.

In addition to reducing the total number of wires, there are three size criteria that have to be met. First, the overall dimensions of the chip should not exceed 1/4 X 1/4 inches. This is a result of placing a flat chip on the curved brain surface. If the chip is too large, the edges will not be in full contact with the brain surface, resulting in lost or erroneous signals. Second, it is theorized that the portion of the brain in interest, the visual cortex, is composed of basic computing elements (BCE) with a diameter of approximately 250 microns. It is this diameter that determines the center to center spacing of the electrodes in the array, which for the present time are established at 250 microns. Third, the size of the electrode surface contacting the brain needs to be varied in order to determine the actual size of the BCE. This is accomplished by maximizing the electrode area and then making the exposed area the desired size by applying polyimide and etching out the unwanted material through a photolithographic process.

The objective of this project then was to design a VLSI nMOS multiplexer within the size limitations, using Stanford University's "Chip Layout Language (CLL)", "UNIX Programmer's Manual", and "2.0 u nMOS Cell Library", and Berkeley University's "CAD Toolbox User's Manual", with the resulting multiplexer being used in conjunction with future generation AFIT brain chip electrode arrays. The need for this multiplexer design arose when it was determined that a JFET multiplexer, previously designed for the brain chip, would not work due to numerous design implementation errors. Since a total redesign of the multiplexer was to be accomplished it was decided to include a feature the previous multiplexer did not have; a selectable counter whose outputs would input to the multiplexer, providing a capability of selecting different sequences of multiplexer selected outputs. In addition, a decision was made to incorporate a nMOS brain chip array with the multiplexer circuitry in the same manner as the original JFET multiplexer was to be incorporated with a JFET brain

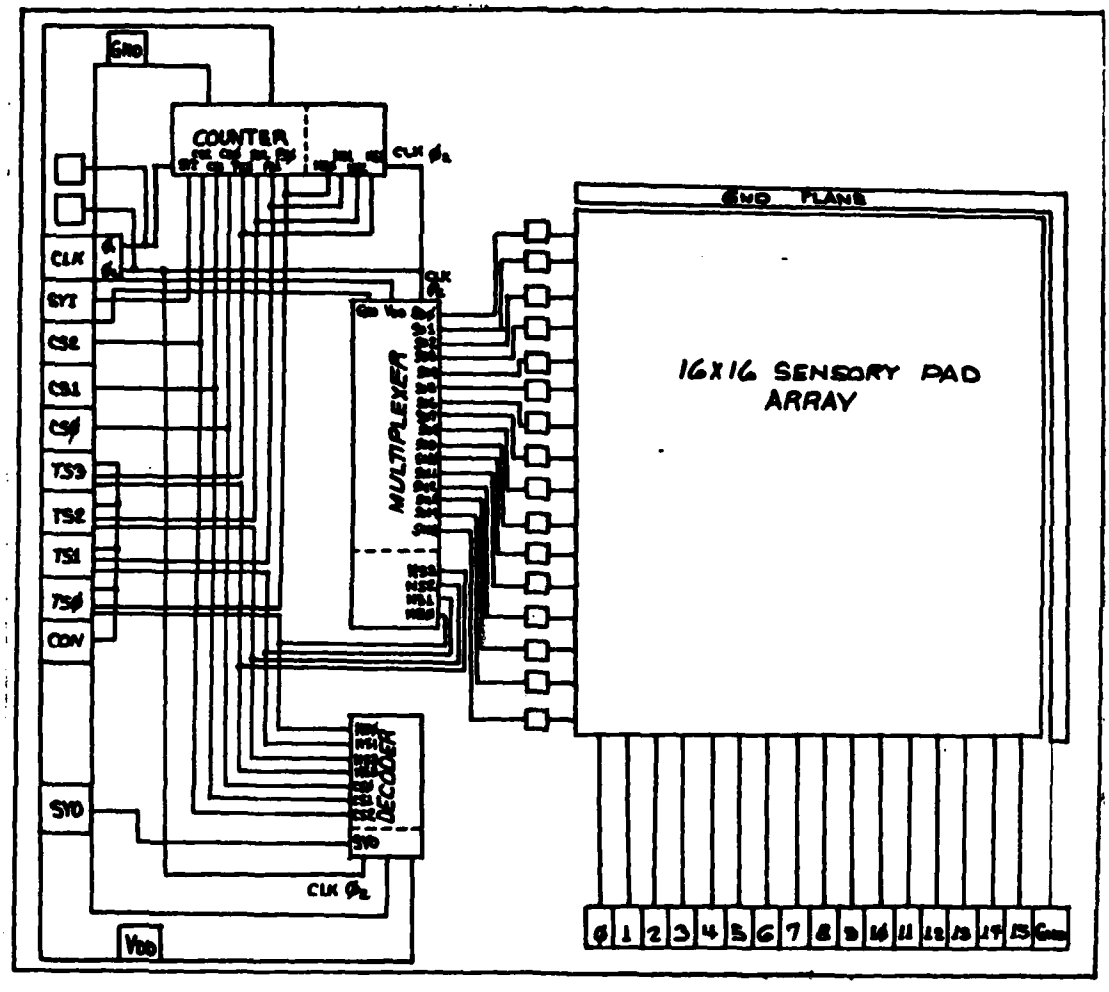


Figure 23. Block Diagram of Brain Chip

chip array. The program that generated the device can be seen in Appendix A, with the resulting plot of the device in Appendix B.

The purpose of this multiplexer is to select one of n-rows of the array, providing m-column outputs. While the multiplexer is designed with sixteen outputs, the count selectability and the basic chip layout allows the user considerable flexibility in the size, number, and type of arrays to be used. Another feature that is presently being designed, but not included in this project, is the multiplexing of the sixteen column outputs, as well as the sixteen rows.

CHIP OPERATION:

The following is a description of how to interface the multiplexer chip to the outside world. Refer to Figure 1, 'Block Diagram of System", and Appendix B, 'CLL Layout", for location of specific pads and operating sections.

POWER AND GROUND PADS: This particular chip can be wired to either 0V to gnd and +5V to Vdd, or -5V to gnd and 0V to Vdd. However, if the multiplexer is detached from the nMOS array and used with a JFET array, gnd must be wired to -5V and Vdd to 0V.

CLOCK PAD: Any single-phase, TTL compatible clock may be input to generate the two-phase, non-inverted, non-overlapping clock signals required to clock the inputs and outputs of the circuitry.

PHASE 1 AND PHASE 2 PADS: These pads allow by-passing the clock input pad, and inputting the two clock phases seperately. This is a "fall-back" design in the event the clock pad does not function properly (see Testing). If the two phases are input through these pads, the clock pad input must be allowed to float.

SYNC IN, AND COUNT STATES 2, 1, AND 0: These pads input the TTL level control signals to the counter and decoder (see block diagram descriptions).

TEST PADS 3, 2, 1, AND 0, AND CONTROL PAD: These are four tri-state buffer pads and their input/output control pad, which are used in testing only (see testing).

SYNC OUT PAD: This pad outputs the sync out signal to an external recording device and provides the sync in input to slave multiplexers, if used (see block diagram description).

BLOCK DIAGRAM DESCRIPTION:

BRAIN CHIP ELECTRODE ARRAY DESIGN AND OPERATION: The brain chip array, or just array, consists of 256 metal electrode pads in a sixteen row by sixteen column matrix, and a ground plane that extends along the top and right hand side of the array. Each pad is connected to its respective column output line through a pass transistor, with each row of pass transistors connected to one of the multiplexer outputs. Whenever one of

the multiplexer lines is selected, that line goes high, turning on all the pass transistors connected to that line. The detected brain signals can then pass along the column output lines to the output pads and on to an external recording device. The ground plane is one long metal pad covering a slightly larger diffused area. With this pad in contact with the brain, the brain and the chip substrate have a common ground plane.

The vertical row of sixteen large pads, between the array and the multiplexer, and the horizontal row of sixteen large pads along the bottom of the array are bonding pads for the array. The seventeenth pad along the bottom is the ground plane bonding pad. In normal use, the bottom row of pads are wired to the outside world, and the vertical row of pads serve no functional purpose. If the user wishes to use a different type of array, however, the chip can be scribed and broken between the vertical row of pads and the array, with the pads now providing a point at which to wire bond the multiplexer outputs to the new array.

The significantly large distance between the vertical row and horizontal row of pads, and the array serves two purposes. First, the vertical row is seperated from the array to allow sufficient room to scribe and break the chip, if desired. Second, once all wires have be connected to the appropriate pads, polyimide (a passivating material) is applied to all exposed pads, except the array pads and ground plane. The polyimide is fluid and will flow slightly until it has set up. The distance between the pads and the array therefore allows enough room for the polyimide to flow without covering the array.

COUNTER DESIGN AND OPERATION: The counter is a finite state machine implemented as a program logic array (PLA), consisting of eight inputs and four outputs. The inputs are sync in (SYI), count state 2 (CS2), count state 1 (CS1), and count state 0 (CS0), plus four output feedback loops which become present state 3 (PS3), present state 2 (PS2), present state 1 (PS1), and present state 0 (PS0). The four outputs, next state 0 (NS0), next state 1 (NS1), next state 2 (NS2), and next state 3 (NS3), in addition to feeding back into the counter PLA, also input to the multiplexer and decoder.

The SYI signal, when low, enables the counter to count through the range determined by the three CS inputs. When SYI is high, the counter is preset to the lowest count of the range determined by the CS inputs. In single multiplexer operation, SYI could be tied low, always enabling the counter, or tied to a signal input, effecting a reset whenever the signal goes high.

In multiple operation, two or more multiplexer chips cascaded in parallel, one chip serves as the master with the other chip(s) as slaves. The master SYI functions as above, with the slave's SYI tied together and connected to the master sync out (described in decoder section). With this configuration, all slaves will be preset to the same count state whenever their SYI goes high. This insures that all slaves will start a selected count sequence in the proper count state.

The CS inputs, in conjunction with SYI and NS inputs, determine what the selected count sequence will be as shown in Table I. A synopsis of Table

I is shown below.

SYI	CS2	CS1	CS0	NS3	NS2	NS1	NS0	COUNTER COUNTS
0	0	0	0	- SEE TABLE I -				0 TO 15
0	0	0	1					0 TO 3
0	0	1	0					4 TO 7
0	0	1	1					8 TO 11
0	1	0	0					12 TO 15
0	1	0	1					0 TO 7
0	1	1	0					8 TO 15
0	1	1	1					0

COUNTER PRESETS

1	0	0	0	X	X	X	X	0
1	0	0	1	X	X	X	X	0
1	0	1	0	X	X	X	X	4
1	0	1	1	X	X	X	X	8
1	1	0	0	X	X	X	X	12
1	1	0	1	X	X	X	X	0
1	1	1	0	X	X	X	X	8
1	1	1	1	X	X	X	X	0

As one can see from Table I, the counter counts sequentially through the count states defined by the CS inputs. The counter will continue counting until SYI goes high (if the option is used), or until a new count sequence is defined by the CS inputs. One can also note that, if the counter is in a count state not within the range of the count sequence, on the next count the next state will be the lowest count state of the defined count sequence.

The counter clocking scheme is to clock the eight inputs into the PLA input buffers during phase 1 (PH1) and to clock the four outputs into the PLA output buffers during phase 2 (PH2). Originally, the counter was designed without clocking the outputs, in order that the signals would propagate through the circuit at maximum speed. It was discovered during testing, however, that the feedback loops were in a race condition and the counter would not count properly. This situation was corrected by adding the clocked output buffers.

DECODER DESIGN AND OPERATION: The decoder is implemented as a PLA consisting of seven inputs and one output. The inputs are NS0, NS1, NS2, and NS3 from the counter PLA, and CS0, CS1, and CS2 from the input signals. The output is sync out (SYO), which goes to an output pad.

The CS and NS inputs determine when the SYO signal goes high, as shown in Table II. Depending on the count sequence, as defined by the CS signals, the SYO goes high whenever the NS inputs are in the highest count state of the defined count sequence.

The SYO performs two functions. First, as a master timing signal to an external recording device, it provides the user with a visual indication between the end of one count sequence and the beginning of the next

count sequence. Second, as mentioned in the counter function, the SYO of a master can be tied to the SYI of any slaves, resulting in all slave counters being forced to a predefined next state, regardless of their present state. This insures that if any slave somehow gets out of the proper count state, it will be forced back into the correct state at the beginning of the next count sequence.

The decoder clocking scheme is simply to clock the SYO into the decoder output buffer during PH2. Since there is no feedback loop in the decoder, not clocking the inputs does not interfere with the proper decoder operation.

MULTIPLEXER DESIGN AND OPERATION: The multiplexer is implemented as a PLA, consisting of four inputs, and sixteen outputs. The inputs are NS0, NS1, NS2, and NS3 from the counter PLA. The outputs are selected out 0 (SO0) through SO15, which go to the respective rows of the brain chip electrode array.

The next state inputs to the multiplexer select the corresponding SO line, as shown in Table III. The selectable count mechanism thus allows the flexibility of selecting what portion of the array are to be monitored. In addition, due to the layout of the chip, one has the capability of seperating the multiplexer side of the chip from the array side (by scribing and breaking), and subsequently using the multiplexer with other arrays of different sizes and technologies (i.e. JFET array with nMOS multiplexer).

The clocking scheme for the multiplexer is similiar to that of the decoder; only the outputs are clocked. Again, with no feedback loops, no problem should arise from not clocking the inputs.

TESTING THE MULTIPLEXER CIRCUITRY:

An important aspect in designing a prototype VLSI circuit is to include components required for testing the various modules and circuitry on the chip. This allows testing without having to place the chip in the particular circuit configuration for which the chip was designed.

The brain chip multiplexer was implemented for testing purposes with four tri-state devices that allows isolating the counter from the decoder and multiplexer. The isolation is accomplished by running the NS wires from the counter PLA, through the tri-state devices, and then to the multiplexer and decoder modules. With a low applied to the tri-state control (CON) pad, the tri-state devices are disabled and appear as an infinite impedance when looking into the input lines. The devices can now be used as input pads. By applying the CS signals is the usual manner, and applying psuedo-NS test signals to the tri-state pads, the operation and output of the multiplexer and decoder can be observed without interference from the counter. With a high applied to CON, the tri-state devices operate normally, and can be used to monitor the NS outputs of the counter PLA.

To test the operation of the chip, Berekley's 'Event Driven Switch Level Simulator (ESIM) was used. When ESIM was first executed, the program

would not return to the interactive mode. This was an indication that some part of the test circuitry was constantly changing. Further indication of the circuit not settling was obtained by interupting the program, and observing the output file. Everything in the output file was undefined. It was suspected, even at this point, that something was wrong with the counter PLA, but at the same time, confidence in running ESIM was not at its highest.

Further testing was performed using ESIM and the tri-state pads as input devices. Under these test conditions, the decoder and multiplexer were found to produce the desired output for any given input. This really got us looking at the counter. Now testing was performed using ESIM and the tri-state pads to monitor the output of the counter PLA. What was observed did not make any sense at all until it was pointed out that the circuit was not settling due to feedback loops being in a race condition. At this point, the counter PLA module was modified to include clocked output buffers (as described earlier), and testing continued. With the addition of the clocked outputs, the counter was now observed to count only the odd (1, 3, 5, etc) states, but at least it was counting. After much thought and frustration, it was felt that the only way this odd count could occur, would be if there was something wrong with the clock pad.

Using ESIM to monitor the output phases of the clock pad, while inputing a clock signal, did not show anything wrong with the clocking mechanism. However, by by-passing the clock pad, and introducing the two clock phases through two added input pads (PH1, PH2), the counter, multiplexer, and decoder were found to operate perfectly. The suspiscions now are that ESIM can not accomadate the two phase clocking mechanism. Somehow it seems that the two phases of the clock pad are both high for a brief period of time when simulated using ESIM. One of the tests to be performed next quarter, will be to input a true TTL clock and observe the the two phases output. It is believed at this point that the clock pad will function as it was designed, and will not create any testing problems. However, should the clock pad prove to be defective, the two pads PH1 and PH2 can be used to input the required clock phases.

The input file to ESIM, and the resulting output file can be seen in Appendices D and E. In addition, the CLL file used to produce the simulation ".cif" file is in Appendix C. This file is different from Appendix A only in the three underlined statements on the first page. A duplicate file was used in the event it got wiped out by some unforeseen mishap.

CONCLUSIONS:

It appears that the multiplexer circuit works as designed,if only through limited static testing using ESIM. Dynamic testing will be performed when fabricated devices are available.

ADVANTAGES OF THE DESIGN: There are two distinct advantages resulting from the way the circuit is designed. First, the multiplexer circuitry can be easily seperated from the brain chip array, and used with other

arrays. While the multiplexer is designed with sixteen output lines, the count selectable feature allows the multiplexer to interface other arrays without modification (except seperating) or additional external hardware. The second advantage is that the counter, decoder, and multiplexer are individual modules, which aided in the troubleshooting isolation. Additionally, by being seperate modules, the three devices were "stacked", thereby requiring less room than if one large PLA containing everything had been designed.

Table VI. Counter PLA Terms

```
\.i 8                /*  Defines 8 inputs to Counter PLA  */
\.o 4                /*  Defines 4 outputs from Counter PLA  */
\.p 119              /*  Defines 119 product terms of Counter PLA  */

   in      out

syi
|cs2
| |cs1
| | |cs0
| | | |ps3
| | | | |ps2
| | | | | |ps1
| | | | | | |ps0
| | | | | | |  ns0
| | | | | | |  |ns1
| | | | | | |  | |ns2
| | | | | | |  | | |ns3
| | | | | | |  | | |
00000000 1000
00000001 0100
00000010 1100
00000011 0010
00000100 1010
00000101 0110
00000110 1110
00000111 0001
00001000 1001
00001001 0101
00001010 1101
00001011 0011
00001100 1011
00001101 0111
00001110 1111
00001111 0000
00010000 1000
00010001 0100
00010010 1100
00010011 0000
00010100 0000
00010101 0000
00010110 0000
00010111 0000
00011000 0000
00011001 0000
00011010 0000
00011011 0000
00011100 0000
00011101 0000
00011110 0000
```

```
00011111 0000
00100000 0010
00100001 0010
00100010 0010
00100011 0010
00100100 1010
00100101 0110
00100110 1110
00100111 0010
00101000 0010
00101001 0010
00101010 0010
00101011 0010
00101100 0010
00101101 0010
00101110 0010
00101111 0010
00110000 0001
00110001 0001
00110010 0001
00110011 0001
00110100 0001
00110101 0001
00110110 0001
00110111 0001
00111000 1001
00111001 0101
00111010 1101
00111011 0001
00111100 0001
00111101 0001
00111110 0001
00111111 0001
01000000 0011
01000001 0011
01000010 0011
01000011 0011
01000100 0011
01000101 0011
01000110 0011
01000111 0011
01001000 0011
01001001 0011
01001010 0011
01001011 0011
01001100 1011
01001101 0111
01001110 1111
01001111 0011
01010000 1000
01010001 0100
01010010 1100
01010011 0010
01010100 1010
01010101 0110
01010110 1110
01010111 0000
01011000 0000
01011001 0000
01011010 0000
```

```
01011011 0000
01011100 0000
01011101 0000
01011110 0000
01011111 0000
01100000 0001
01100001 0001
01100010 0001
01100011 0001
01100100 0001
01100101 0001
01100110 0001
01100111 0001
01101000 1001
01101001 0101
01101010 1101
01101011 0011
01101100 1011
01101101 0111
01101110 1111
01101111 0001
1000---- 0000
1001---- 0000
1010---- 0010
1011---- 0001
1100---- 0011
1101---- 0000
1110---- 0001
\.e                    /*  Defines the end of the file  */
%
```

Table VII. Decoder PLA terms

```
\.i 7                   /*  Defines 7 inputs to Decoder PLA  */
\.o 1                   /*  Defines 1 output from Decoder PLA  */
\.p 7                   /*  Defines 7 product terms of Decoder PLA  */

   in   out

ns0
|ns1
| |ns2
| | |ns3
| | | |cs2
| | | | |cs1
| | | | | |cs0
| | | | | | |
| | | | | | |sys0
| | | | | | | |
1111000 1
1100001 1
1110010 1
1101011 1
1111100 1
1110101 1
1111110 1
\.e                     /*  Defines the end of the file  */
%
```

Table VIII. Multiplexer PLA Terms

```
\.i 4                   /*  Defines 4 inputs to Multiplexor PLA  */
\.o 16                  /*  Defines 16 outputs from Multiplexor PLA  */
\.p 16                  /*  Defines 16 product terms of Multiplexor PLA  */

 in          out

ns0
 ns1
  ns2
   ns3
     so15
      so14
       so13
        so12
         so11
          so10
           so9
            so8
             so7
              so6
               so5
                so4
                 so3
                  so2
                   so1
                    so0
0000 0000000000000001
1000 0000000000000010
0100 0000000000000100
1100 0000000000001000
0010 0000000000010000
1010 0000000000100000
0110 0000000001000000
1110 0000000010000000
0001 0000000100000000
1001 0000001000000000
0101 0000010000000000
1101 0000100000000000
0011 0001000000000000
1011 0010000000000000
0111 0100000000000000
1111 1000000000000000
\.e                     /*  Defines the end of the file  */
%
```

Computer Listing for the Non-multiplexed Output Brain Chip

```
project.cll
/*************************************************************
This cll program generates the cll plot for the single multi-
plexer chip.  To run this particular program, type:

cll <switch options> project.cll comb_pla.cif


*************************************************************/
/*  Include external definitions for library cells  */

#include "/usr/lib/local/s_ext.cll"

/*  Define external reference to pla 981, 982, 983  */

external a981 (cif 981 bounds --15,0 164,65)  /*  Decoder  */
external a982 (cif 982 bounds --15,0 236,145)  /*  Multiplexer  */
external a983 (cif 983 bounds --15,0 284,311)  /*  Counter  */

brain_chip

{

wire poly --467,--427 w 2 u 2;
wire poly 3818,2766 w 2 u 2;

/*  Insert the 16 X 16 brain chip electrode array  */


iterate 16,16 125,125
  electrode (1150,640);

/*  Insert the brain chip row select bonding pads  */

iterate 1,16 641,125
  r_bonding_pads (589,661);

/*  Insert the brain chip column output and ground plane
    bonding pads                                          */

iterate 17,1 125,641
  c_bonding_pads (1150,0);

/*  Insert the brain chip ground plane  */

wire diff 3154,640 w 8 u 4 r 7;
wire diff 3210.5,640 w 115 u 2867.5 l 2860.5;
wire cut 3210.5,641 w 115 u 2866.5 l 2859.5;
wire metal 3210.5,640 w 115 u 2867.5 l 2860.5;
wire glass 3210.5,641 w 115 u 2866.5 l 2859.5;

/*  Insert the input, output, vdd, and gnd pads  */

/*  Insert the tri-state control signal pad  */
```

```
iterate 1,1 152,100
  NIn8 (0,1500 rotate 3);

/*  Connect control pad output to tri-state pads  */

wire metal 152,1505 w 4 r 50 u 400;  /*  Control signal bus  */
wire poly 170,1485 w 2 r 12
  metal w 4 d 2;  /*  Tri-State 0 (TS0) to control signal bus  */
wire poly 170,1585 w 2 r 12
  metal w 4 d 2;  /*  Tri-State 1 (TS1) to control signal bus  */
wire poly 170,1685 w 2 r 12

metal w 4 d 2;  /*  Tri-State 2 (TS2) to control signal bus  */
wire poly 170,1785 w 2 r 12
  metal w 4 d 2;  /*  Tri-State 3 (TS3) to control signal bus  */

/*  Insert the tri-state test pads  */

iterate 1,4 170,100
  NTriState8 (0,1400 rotate 3 flip ud);

/*  Insert the Counter input signals (Sync In, CS2, CS1, CS0) pads  */

iterate 1,4 152,100
  NIn8 (0,1800 rotate 3);

/*  Connect signal input pads to Counter and Decoder inputs  */

wire diff 189,2283 w 2 d 2
  metal w 4 d 176 l 57;  /*  Sync In (SYI) to Counter  */
wire diff 205,2283 w 2 d 2
  metal w 4 d 276 l 73;  /*  Control Select 2 (CS2) to Counter  */
wire diff 221,2283 w 2 d 2
  metal w 4 d 376 l 89;  /*  Control Select 1 (CS1)  to Counter  */
wire diff 237,2283 w 2 d 2
  metal w 4 d 476 l 105;  /*  Control Select 0 (CS0) to Counter  */
wire diff 122,2005 w 4 r 155
  metal w 4 d 755 l 130 d 23
  diff w 4 d 22
  metal w 4 d 356 r 45 d 74 r 65
  poly w 2 r 5;  /*  Control Select 2 (CS2) to Decoder  */
wire diff 122,1905 w 4 r 139
  metal w 4 d 635 l 128 d 43
  diff w 4 d 22
  metal w 4 d 366 r 49 d 80 r 75
  poly w 2 r 5;  /*  Control Select 1 (CS1) to Decoder  */
wire diff 122,1805 w 4 r 123
  metal w 4 d 515 l 126 d 63
  diff w 4 d 22
  metal w 4 d 376 r 53 d 86 r 85
  poly w 2 r 5;  /*  Control Select 0 (CS0) to Decoder  */

/*  Insert the non-inverting two-phase clock pad  */
```

```
iterate 1,1 179,100
  NClk (0,2200 rotate 3);


/*  Connect phase two to Counter, Multiplexer, and Decoder clocked
    outputs                                                        */

wire metal 177,2228 w 4 r 2
  poly 179,2228 w 4 r 129 d 2
  metal w 4 d 994
  poly w 2 d 4 r 7 d 5;  /*  Phase 2 (PH2) to Multiplexer  */
wire poly 308,2228 w 4 r 52 u 111 l 8;  /* Phase 2 (PH2) to Counter  */
wire poly 315,1087 w 4 d 10 r 50
  metal w 4 r 25 d 384
  poly w 4 l 87 u 7;  /*  Phase 2 (PH2) to Decoder  */

/*  Insert Phase 1 (PH1) and Phase 2 (PH2) external bonding pads  */

iterate 1,2 106,100
  NBlank (0,2300 rotate 3);

/*  Connect Phase 1 (PH1) external bonding pad to Phase 1 (PH1).
    internal  */

wire metal 77.5,2350 w 4 r 2
  diff w 4 r 50.5 d 56 r 47 d 8
  poly w 2 d 2;  /*  Phase 1 (PH1)  */

/*  Connect Phase 2 (PH2) external bonding pad to Phase 2 (PH2)
    internal  */

wire metal 77.5,2450 w 4 r 2
  diff w 4 r 33.5
  metal w 4 r 27 d 145 r 30 d 42;  /*  Phase 2 (PH2)  */

/*  Insert the Decoder output signal (Sync Out) pad  */

iterate 1,1 145,100
  NOut8 (0,700 rotate 3);

/*  Insert the ground pad  */

iterate 1,1 100,106
  NGnd (200,2660 rotate 6);

/*  Connect all pads' ground  */

wire metal 200,2660 w 16 l 102 d 2570 r 202;

/*  Insert the vdd pad  */

iterate 1,1 100,80
  NVdd (200,0);

/*  Connect all pads' vdd  */
```

```
wire metal 200,4 w 8 l 196 u 2758 r 196;

/*  Insert the counter, multiplexer, and decoder plas  */

iterate 1,1

  counter (164,2260);

/*  Connect Counter outputs to tri-state inputs, and tri-state
    outputs to Multiplexer and Decoder inputs                    */

wire metal 253,2260 w 4 d 539
  diff w 4 l 83
  poly w 2 l 2;  /*  Counter Next State 3 (NS3) to Tri-State 3 (TS3)
                     input  */
wire metal 168,1704 w 3 r 2
  diff w 4 r 83
  metal w 4 d 424 l 127 d 53
  diff w 4 d 22
  metal w 4 d 251
  diff w 4 r 78 d 7
  metal w 4 d 156 r 53
  poly w 2 r 5;  /*  Tri-State 3 (TS3) output to Decoder input  */
wire metal 269,2267 w 4 d 646
  diff w 4 l 99
  poly w 2 l 2;  /*  Counter Next State 2 (NS2) to Tri-State 2 (TS2)
                     input  */

wire metal 168,1604 w 3 r 2
  diff w 4 r 99
  metal w 4 d 344 l 129 d 33
  diff w 4 d 22
  metal w 4 d 241
  diff w 4 r 74 d 17
  metal w 4 d 140 r 43
  poly w 2 r 5;  /*  Tri-State 2 (TS2) output to Decoder input  */
wire metal 285,2274 w 4 d 753
  diff w 4 l 115
  poly w 2 l 2;  /*  Counter Next State 1 (NS1) to Tri-State 1 (TS1)
                     input  */
wire metal 168,1504 w 3 r 2
  diff w 4 r 115
  metal w 4 d 264 l 131 d 13
  diff w 4 d 22
  metal w 4 d 231
  diff w 4 r 70 d 27
  metal w 4 d 124 r 33
  poly w 2 r 5;  /*  Tri-State 1 (TS1) output to Decoder input  */
wire metal 301,2281 w 4 d 860
  diff w 4 l 131
  poly w 2 l 2;  /*  Counter Next State 0 (NS0) to Tri-State 0 (TS0)
                     input  */
wire metal 168,1404 w 3 r 2
  diff w 4 r 131
  metal w 4 d 174 l 140 d 3
```

```
  diff w 4 d 22
  metal w 4 d 221
  diff w 4 r 73 d 37
  metal w 4 d 108 r 23
  poly w 2 r 5;  /*  Tri-State 0 (TS0) output to Decoder input  */
wire diff 232,984 w 4 r 2
  metal w 4 r 121 u 36
  poly w 2 l 3;  /*  Tri-State 3 (TS3) output to Multiplexer  */
wire diff 222,974 w 4 r 2
  metal w 4 r 138 u 62 l 7
  poly w 2 l 3;  /*  Tri-State 2 (TS2) output to Multiplexer  */

wire diff 212,964 w 4 r 2
  metal w 4 r 155 u 88 l 14
  poly w 2 l 3;  /*  Tri-State 1 (TS1) output to Multiplexer  */
wire diff 202,954 w 4 r 2
  metal w 4 r 172 u 114 l 21
  poly w 2 l 3;  /*  Tri-State 0 (TS0) output to Multiplexer  */

/*  Connect Counter to vdd and gnd  */

wire metal 349,2652 w 4 u 108 l 49;  /*  Vdd  */
wire metal 357,2637 w 4 u 25
  diff w 4 l 17
  metal w 4 l 40;  /*  Gnd  */

iterate 1,1 248,213
  multiplexer (170,995 rotate 9);

/*  Connect Multiplexer outputs to brain chip row select pads  */

wire poly 366,1210 w 2 r 4
  metal w 4 r 20 u 1328 r 119;  /*  Select Out 0 (SO0) to row 0  */
wire poly 366,1202 w 2 r 4
  metal w 4 r 30 u 1211 r 109;  /*  Select Out 1 (SO1) to row 1  */
wire poly 366,1194 w 2 r 4
  metal w 4 r 40 u 1094 r 99;  /*  Select Out 2 (SO2) to row 2  */
wire poly 366,1186 w 2 r 4
  metal w 4 r 50 u 977 r 89;  /*  Select Out 3 (SO3) to row 3  */
wire poly 366,1178 w 2 r 4
  metal w 4 r 60 u 860 r 79;  /*  Select Out 4 (SO4) to row 4  */
wire poly 366,1170 w 2 r 4
  metal w 4 r 70 u 743 r 69;  /*  Select Out 5 (SO5) to row 5  */
wire poly 366,1162 w 2 r 4
  metal w 4 r 80 u 626 r 59;  /*  Select Out 6 (SO6) to row 6  */
wire poly 366,1154 w 2 r 4
  metal w 4 r 90 u 509 r 49;  /*  Select Out 7 (SO7) to row 7  */
wire poly 366,1146 w 2 r 4
  metal w 4 r 100 u 392 r 39;  /*  Select Out 8 (SO8) to row 8  */

wire poly 366,1138 w 2 r 4
  metal w 4 r 110 u 275 r 29;  /*  Select Out 9 (SO9) to row 9  */
wire poly 366,1130 w 2 r 4
  metal w 4 r 120 u 158 r 19;  /*  Select Out 10 (SO10) to row 10  */
```

```
wire poly 366,1122 w 2 r 4
  metal w 4 r 130 u 41 r 9;  /*  Select Out 11 (SO11) to row 11  */
wire poly 366,1114 w 2 r 4
  metal w 4 r 130 d 76 r 9;  /*  Select Out 12 (SO12) to row 12  */
wire poly 366,1106 w 2 r 4
  metal w 4 r 120 d 193 r 19;  /*  Select Out 13 (SO13) to row 13  */
wire poly 366,1098 w 2 r 4
  metal w 4 r 110 d 310 r 29;  /*  Select Out 14 (SO14) to row 14  */
wire poly 366,1090 w 2 r 4
  metal w 4 r 100 d 427 r 39;  /*  Select Out 15 (SO15) to row 15  */

/*  Connect Multiplexer to vdd and gnd  */

wire metal 170,1212 w 4 l 59

  diff w 4 l 26
  metal w 4 l 77;  /*  Vdd  */
wire metal 185,1220 w 4 l 79;  /*  Gnd  */

iterate 1,1 184,153
  decoder (250,700 rotate 3);

/*  Connect Decoder output (SYO) to output pad  */

wire poly 252,721 w 2 l 2
  metal w 4 l 90 u 29 l 10
  poly w 2 l 5;

/*  Connect Decoder to vdd and gnd  */

wire metal 343,701 w 16 d 603 l 43;  /*  Gnd  */
wire metal 364,708 w 4 d 4 w 8 d 700 l 64;  /*  Vdd  */

}

/*************************************************************

     This is the program that lays out the brain chip array
(16 X 16) as it interfaces with the multiplexer, and the
outside world.

*************************************************************/

electrode

{

/*  Build the brain chip electrode  */

wire metal 21.5,80 w 90 r 90;
rect 22.5,36 88,88 glass;
wire metal 66.5,35 w 10 d 6;
wire diff 66.5,33 w 10 d 19 w 8 l 9;
wire metal 61.5,14 w 8 l 57.5 d 14 u 125;
```

```
rect 58.5,11 2,6 contact;
rect 62.5,30 8,2 contact;
wire diff 0,25 w 4 r 15 metal w 4 r 43.5
     poly w 4 r 20 metal w 4 r 43.5 diff w 4 r 5;

)

r_bonding_pads

(

/*  Build the brain chip bonding pad  */

wire diff 0,25 w 4 l 5
  metal w 4 l 636;
rect --640,25 115,111 metal;
rect --639,22 113,113 glass;

)

c_bonding_pads

(

/*  Build the brain chip column output bonding pads  */

wire metal 4,0 w 8 u 645;
rect 8,0 107,115 metal;
rect 1,1 113,113 glass;

)

/*****************************************************************

     This is the program that generates the Counter PLA,
with its clocked input "register" and unclocked ouput
"register".  This PLA has eight inputs and four outputs.

*****************************************************************/

counter

(

/*  Make the Counter Pla with input and output buffers  */

a903 (20,20);

/* Insert the PlaClockIn modules, which make clocked input register  */

iterate 8,1 16,58
  PlaClockIn (35,--38);
```

```
/*  Insert the PlaClockOut modules, which make the clocked output
   register  */

iterate 2,1 16,53
  PlaClockOut (176,--33);

/*  Connect PLA Vdd and drivers Vdd, and PLA Gnd and drivers Gnd  */

wire metal 22,20 w 4 d 22 r 13;
wire metal 163,--2 w 4 r 5 d 21 r 8;
wire metal 163,17 w 4 r 10 u 3 d 15 r 8;
wire metal 208,5 w 4 r 5 u 15;

/*  Connect feed back lines  */

wire diff 109,--38 w 2 d 20 r 94 u 20
  poly w 2 u 5;  /*  Present State 3 (PS3) to Next State 3 (NS3)  */
wire diff 109,--56 w 2 d 2
  metal w 4 d 3;  /*  Extend PS3  */
wire diff 125,--38 w 2 d 14 r 70 u 15
  poly w 2 u 4;  /*  Present State 2 (PS2) to Next State 2 (NS2)  */

wire diff 125,--50 w 2 d 2
  metal w 4 d 3;  /*  Extend PS2  */
wire diff 141,--38 w 2 d 8 r 46 u 8
  poly w 2 u 5;  /*  Present State 1 (PS1) to Next State 1 (NS1)  */
wire diff 141,--44 w 2 d 2
  metal w 4 d 3;  /*  Extend PS1  */
wire diff 157,--38 w 2 d 2 r 22 u 7
  poly w 2 u 2;  /*  Present State 0 (PS0) to Next State 0 (NS0)  */
wire diff 157,--38 w 2 d 2
  metal w 4 d 3;  /*  Extend PS0  */
}

/*********************************************************

    This is the program that makes the Decoder PLA,
with its unclocked input "register" and clocked output
"register".  This PLA has seven inputs and one output.

*********************************************************/

decoder

{

/*  Make Decoder Pla with input and output buffers  */

a901 (20,20);

/*  Insert the PlaIn modules, which make unclocked input register  */

iterate 7,1 16,41
  PlaIn (35,--21);
```

```
/*Insert the PlaClockOut module, which makes clocked output register */

iterate 1,1 16,57
  PlaClockOut (160,--33);

/*  Connect PLA Vdd and drivers Vdd, and PLA Gnd and drivers Gnd  */

wire metal 22,20 w 4 d 22 r 13;
wire metal 147,--2 w 4 r 5 d 21 r 8;
wire metal 147,17 w 4 r 10 u 3 d 15 r 8;
wire metal 176,5 w 4 r 5 u 15;
wire poly 176,18 w 2 r 8;

}

/*************************************************************

     This is the program that generates the Multiplexer PLA,
with its unclocked input "register" and clocked output
"register".  This PLA has four inputs and sixteen outputs.

*************************************************************/

multiplexer

{

/*  Make Multiplexer Pla with input and output buffers  */

a902 (20,20);

/*  Insert the PlaIn modules, which make unclocked input register  */

iterate 4,1 16,41
  PlaIn (35,--21);

/*Insert the PlaClockOut modules, which make clocked output register */

iterate 8,1 16,57
  PlaClockOut (112,--33);

/*  Connect PLA Vdd and drivers Vdd, and PLA Gnd and drivers Gnd  */

wire metal 22,20 w 4 d 22 r 13;
wire metal 99,--2 w 4 r 5 d 21 r 8;
wire metal 99,17 w 4 r 10 u 3 d 15 r 8;
wire metal 240,5 w 4 r 5 u 15;
wire poly 240,18 w 2 r 8;

}
```

Computer Listing for the Multiplexed Output Brain Chip

```
projectd.cll

/*************************************************************
This cll program generates the cll plot for the double multi-
plexer chip.  To use this program, type:

cll <switch options> projectd.cll comd_pla.cif clkpad.cif

*************************************************************/
/*  Include external definitions for library cells  */

#include "/usr/lib/local/s_ext.cll"

/*  Define external reference to pla 901, 902, 903, and modclock 904 */

external a901 (cif 901 bounds --15,0 180,63)  /*  Decoder  */
external a902 (cif 902 bounds --15,0 236,143)  /*  Multiplexer  */
external a903 (cif 903 bounds --15,0 204,311)  /*  Counter  */
external a904 (cif 904 bounds 0,0 100,179)  /*  Modified NClk pad  */

brain_chip

{

wire poly --391,99 w 2 u 2;
wire poly 3565,2310 w 2 u 2;

/*  Insert the 16 X 16 brain chip electrode array  */

iterate 16,16 125,125
  electrode (447,640);

/*  Insert the column output pad and ground plane pad  */

iterate 1,2 125,125
  c_bonding_pads (0,456);

/*  Insert the brain chip ground plane and connect to pad  */

wire diff 2507.5,647 w 115 u 2060.5 l 2060.5;
wire cut 2507.5,648 w 113 u 2059.5 l 2059.5;
wire metal 2507.5,647 w 115 u 2060.5 l 2060.5;
wire glass 2507.5,648 w 113 u 2059.5 l 2059.5;
wire metal 115,464 w 16 r 2343 u 183;

/*  Insert the column output lines and connect to the output pad  */

iterate 16,1 125,156
  lines (447,488);

wire metal 115,589 w 16 r 13 d 105 r 2202;

/*  Insert the vdd pad  */
```

```
iterate 1,1 80,100
  NVdd (0,740 rotate 3);

/*  Insert the ground pad  */

iterate 1,1 100,106
  NGnd (240,2660 rotate 6);

/*  Insert the input signals (Sync In, CS2, CS1, CS0) pads  */

iterate 1,4 132,100
  NIn8 (0,1800 rotate 3);

/*  Insert the Decoder output signal (Sync Out) pad  */
iterate 1,1 145,100
  NOut8 (0,1264 rotate 3);

/*  Insert the two non-inverting two-phase clock pads  */

iterate 1,1 179,100
  a904 (0,2200 rotate 3);

iterate 1,1 179,100
  NClk (0,840 rotate 3 flip ud);

/*  Insert the Counter, Multiplexers, and Decoder PLAs  */

iterate 1,1
  counter (164,2260);

iterate 1,1 248,213
  multiplexer (170,1495 rotate 9);

iterate 1,1 248,213
  multiplexer (150,494 rotate 9 flip ud);

iterate 1,1 184,133
  decoder (250,1264 rotate 3);

/*  Insert the four-bit Counter  */

iterate 4,1 24,115
  Cnt (260,810.5);

/*  Insert the dummy counter cell (Count Restore)  */

iterate 1,1 44,115
  CntRestore (216,810.5);

/*  Insert the Inverting Super Buffer and connect to the Modclk  */

iterate 1,1 46,20
  RInv8B8 (26,2210 rotate 3);
```

```
wire diff 72,2220 w 2 r 5 w 4 d 13 r 3;

/*  Connect all the pads to vdd  */

wire metal 4,840 w 8 u 1922 r 236;

/*  Connect all the pads to ground  */

wire metal 240,2668 w 16 l 142 d 1928;

/*  Connect the Counter to vdd and gnd  */

wire metal 349,2652 w 4 u 110 w 8 l 9;  /*  Vdd  */
wire metal 357,2657 w 4 u 25
  diff w 4 l 19
  metal w 4 l 2;  /*  Gnd  */

/*  Connect the Multiplexer to vdd and gnd  */

wire metal 170,1712 w 4 l 59
  diff w 4 l 26
  metal w 4 l 77;  /*  Vdd  */
wire metal 185,1720 w 4 l 79;  /*  Gnd  */

/*  Connect the Decoder to vdd and gnd  */

wire metal 364,1272 w 4 d 19 l 253
  diff w 4 l 26
  metal w 4 l 77;  /*  Vdd  */
wire metal 345,1265 w 4 d 5 l 239;  /*  Gnd  */

/*  Connect the 4-bit Counter to vdd and gnd  */

wire metal 356,850.5 w 4 r 12 u 75 l 12 r 12 u 26.5 l 257
  diff w 4 l 26
  metal w 4 l 77;  /*  Vdd  */
wire metal 356,869.5 w 4 r 5 u 47
  diff w 4 u 14
  metal w 4 u 12.5 l 255;  /*  Gnd  */

/*  Connect 4-bit Counter Carry-in to Vdd and NOT Carry-in to Gnd  */

wire metal 204,952 w 4 d 2
  diff w 4 d 14
  metal w 4 d 44 w 3 r 12;  /*  Carry-in  */
wire metal 211,941 w 4 d 34 w 3 r 5;  /*  NOT Carry-in  */

/*  Connect the Multiplexer 2 to vdd and gnd  */

wire metal 154,728 w 4 l 2
  diff w 4 l 67
  metal w 8 l 81 u 12;  /*  Vdd  */
wire diff 157,709 w 4 l 19
  metal w 4 l 40 w 16 u 31;  /*  Gnd  */
```

```
/*  Connect the Inverting Super Buffer to vdd and gnd  */

wire metal 69,2238 w 6 u 5 w 4 l 27 d 5 u 5 l 34;  /*  Vdd  */
wire diff 58,2238 w 6 u 57 w 4 r 34
  metal w 4 r 2;  /*  Gnd  */

/*  Connect signal input pads to Counter and Decoder inputs  */

wire diff 189,2285 w 2 d 2
  metal w 4 d 176 l 57;  /*  Sync In (SYI) to Counter  */
wire diff 205,2285 w 2 d 2
  metal w 4 d 276 l 73;  /*  Control Select 2 (CS2) to Counter  */
wire diff 221,2285 w 2 d 2
  metal w 4 d 376 l 89;  /*  Control Select 1 (CS1) to Counter  */
wire diff 237,2285 w 2 d 2
  metal w 4 d 476 l 105;  /*  Control Select 0 (CS0) to Counter  */
wire metal 205,2005 w 4 r 2
  diff w 4 r 72
  metal w 4 d 255 l 130 d 23
  diff w 4 d 22
  metal w 4 d 276 r 43 d 74 r 68
  poly w 2 r 4;  /*  Control Select 2 (CS2) to Decoder  */
wire metal 219,1905 w 4 r 2
  diff w 4 r 40
  metal w 4 d 135 l 128 d 43
  diff w 4 d 22
  metal w 4 d 286 r 47 d 80 r 78
  poly w 2 r 4;  /*  Control Select 1 (CS1) to Decoder  */
wire metal 237,1805 w 4 r 8 d 15 l 126 d 63
  diff w 4 d 22
  metal w 4 d 296 r 51 d 86 r 88
  poly w 2 r 4;  /*  Control Select 0 (CS0) to Decoder  */

/*  Connect the Counter outputs to Multiplexer and Decoder inputs  */

wire metal 253,2260 w 4 d 480 l 127 d 53
  diff w 4 d 22
  metal w 4 d 251
  diff w 4 r 76 d 7
  metal w 4 d 76 r 56
  poly w 2 r 4;  /*  Counter Next State 3 (NS3) output to Decoder
                     input  */
wire metal 269,2267 w 4 d 507 l 129 d 55
  diff w 4 d 22
  metal w 4 d 241
  diff w 4 r 72 d 17
  metal w 4 d 60 r 46
  poly w 2 r 4;  /*  Counter Next State 2 (NS2) output to Decoder
                     input  */
wire metal 285,2274 w 4 d 534 l 131 d 13
  diff w 4 d 22
  metal w 4 d 251
  diff w 4 r 68 d 27
  metal w 4 d 44 r 36
```

```
  poly w 2 r 4;  /*  Counter Next State 1 (NS1) output to Decoder
                     input  */
wire metal 301,2281 w 4 d 551 l 140 d 5
  diff w 4 d 22
  metal w 4 d 221
  diff w 4 r 71 d 37
  metal w 4 d 28 r 26
  poly w 2 r 4;  /*  Counter Next State 0 (NS0) output to Decoder
                     input  */
wire diff 230,1484 w 4 r 2
  metal w 4 r 125 u 36
  poly w 2 l 5;  /* Counter Next State 3 (NS3) output to Multiplexer */
wire diff 220,1474 w 4 r 2
  metal w 4 r 142 u 62 l 7
  poly w 2 l 5;  /* Counter Next State 2 (NS2) output to Multiplexer */
wire diff 210,1464 w 4 r 2
  metal w 4 r 159 u 88 l 14
  poly w 2 l 5;  /* Counter Next State 1 (NS1) output to Multiplexer */
wire diff 200,1454 w 4 r 2
  metal w 4 r 176 u 114 l 21
  poly w 2 l 5;  /* Counter Next State 0 (NS0) output to Multiplexer */

/*  Connect the 4-bit Counter outputs to Multiplexer 2 inputs  */

wire metal 281,810.5 w 4 d 73.5 r 55 d 32
  poly w 2 l 2;
wire metal 305,810.5 w 4 d 66.5 r 38 d 55 l 7
  poly w 2 l 2;
wire metal 329,810.5 w 4 d 59.5 r 21 d 78 l 14
  poly w 2 l 2;
wire metal 353,810.5 w 4 d 52.5 r 4 d 101 l 21
  poly w 2 l 2;

/*  Connect 4-bit Counter MSB to Modclk input  */

wire diff 353,812.5 w 4 r 31
  metal w 4 u 634.5
  diff w 4 u 275 l 21
  metal w 4 u 15 l 48 u 462
  diff w 4 l 168
  poly w 4 l 123 u 27;

/*  Connect the Multiplexer outputs to the brain chip rows  */

wire poly 366,1710 w 2 r 4
  metal w 4 u 828 r 72
  diff w 4 r 5;  /*  Select Out 0 (SO0) to row 0  */
wire poly 366,1702 w 2 r 4
  metal w 4 r 7 u 711 r 65
  diff w 4 r 5;  /*  Select Out 1 (SO1) to row 1  */
wire poly 366,1694 w 2 r 4
  metal w 4 r 14 u 594 r 58
  diff w 4 r 5;  /*  Select Out 2 (SO2) to row 2  */
```

```
wire poly 366,1686 w 2 r 4
  metal w 4 r 21 u 477 r 51
  diff w 4 r 5;  /*  Select Out 3 (S03) to row 3  */
wire poly 366,1678 w 2 r 4
  metal w 4 r 28 u 360 r 44
  diff w 4 r 5;  /*  Select Out 4 (S04) to row 4  */
wire poly 366,1670 w 2 r 4
  metal w 4 r 35 u 243 r 37
  diff w 4 r 5;  /*  Select Out 5 (S05) to row 5  */
wire poly 366,1662 w 2 r 4
  metal w 4 r 42 u 126 r 30
  diff w 4 r 5;  /*  Select Out 6 (S06) to row 6  */
wire poly 366,1654 w 2 r 4
  metal w 4 r 49 u 9 r 23
  diff w 4 r 5;  /*  Select Out 7 (S07) to row 7  */
wire poly 366,1646 w 2 r 4
  metal w 4 r 70 d 108 r 2
  diff w 4 r 5;  /*  Select Out 8 (S08) to row 8  */
wire poly 366,1638 w 2 r 4
  metal w 4 r 63 d 225 r 9
  diff w 4 r 5;  /*  Select Out 9 (S09) to row 9  */
wire poly 366,1630 w 2 r 4
  metal w 4 r 56 d 342 r 16
  diff w 4 r 5;  /*  Select Out 10 (S010) to row 10  */
wire poly 366,1622 w 2 r 4
  metal w 4 r 49 d 459 r 23
  diff w 4 r 5;  /*  Select Out 11 (S011) to row 11  */
wire poly 366,1614 w 2 r 4
  metal w 4 r 42 d 576 r 30
  diff w 4 r 5;  /*  Select Out 12 (S012) to row 12  */
wire poly 366,1606 w 2 r 4
  metal w 4 r 35 d 693 r 37
  diff w 4 r 5;  /*  Select Out 13 (S013) to row 13  */
wire poly 366,1598 w 2 r 4
  metal w 4 r 28 d 810 r 44
  diff w 4 r 5;  /*  Select Out 14 (S014) to row 14  */
wire poly 366,1590 w 2 r 4
  metal w 4 r 21 d 927 r 51
  diff w 4 r 5;  /*  Select Out 15 (S015) to row 15  */

/*  Connect the Multiplexer 2 outputs to the brain chip columns  */

wire poly 346,515 w 2 r 4
  metal w 4 r 92
  poly w 4 r 15;  /*  Selected Out 0 (2S00) to column 0  */
wire poly 346,523 w 2 r 4
  metal w 4 r 217
  poly w 4 r 15;  /*  Selected Out 1 (2S01) to column 1  */
wire poly 346,531 w 2 r 4
  metal w 4 r 342
  poly w 4 r 15;  /*  Selected Out 2 (2S02) to column 2  */
wire poly 346,539 w 2 r 4
  metal w 4 r 467
  poly w 4 r 15;  /*  Selected Out 3 (2S03) to column 3  */
```

```
wire poly 346,547 w 2 r 4
  metal w 4 r 592
  poly w 4 r 15;  /*  Selected Out 4 (2S04) to column 4  */
wire poly 346,555 w 2 r 4
  metal w 4 r 717
  poly w 4 r 15;  /*  Selected Out 5 (2S05) to column 5  */

wire poly 346,563 w 2 r 4
  metal w 4 r 842
  poly w 4 r 15;  /*  Selected Out 6 (2S06) to column 6  */
wire poly 346,571 w 2 r 4
  metal w 4 r 967
  poly w 4 r 15;  /*  Selected Out 7 (2S07) to column 7  */
wire poly 346,579 w 2 r 4
  metal w 4 r 1092
  poly w 4 r 15;  /*  Selected Out 8 (2S08) to column 8  */
wire poly 346,587 w 2 r 4
  metal w 4 r 1217
  poly w 4 r 15;  /*  Selected Out 9 (2S09) to column 9  */
wire poly 346,595 w 2 r 4
  metal w 4 r 1342
  poly w 4 r 15;  /*  Selected Out 10 (2S010) to column 10  */
wire poly 346,603 w 2 r 4
  metal w 4 r 1467
  poly w 4 r 15;  /*  Selected Out 11 (2S011) to column 11  */
wire poly 346,611 w 2 r 4
  metal w 4 r 1592
  poly w 4 r 15;  /*  Selected Out 12 (2S012) to column 12  */
wire poly 346,619 w 2 r 4
  metal w 4 r 1717
  poly w 4 r 15;  /*  Selected Out 13 (2S013) to column 13  */
wire poly 346,627 w 2 r 4
  metal w 4 r 1842
  poly w 4 r 15;  /*  Selected Out 14 (2S014) to column 14  */
wire poly 346,635 w 2 r 4
  metal w 4 r 1967
  poly w 4 r 15;  /*  Selected Out 15 (2S015) to column 15  */

/*  Connect the Multiplexer 2 Select Out 15 (2S015) to the Decoder  */

wire metal 377,637 w 4 u 608 l 136
  diff w 4 u 62 r 17
  poly w 2 r 4;

/*  Connect the Decoder Sync Out (SYO) to the output pad  */

wire poly 252,1285 w 2 l 2
  metal w 4 l 98 u 29 l 12
  poly w 2 l 5;

/*  Connect phase one of the MClk to phase one of the 4-bit Counter  */

wire metal 177,852 w 4 d 35.5 r 57
  poly w 2 r 2;
```

```
/*  Connect phase two of the NClk to phase 2 of the 4-bit Counter  */

wire metal 179,912 w 4 r 8 d 36 w 3 r 29;

/* Connect phase two of the NClk to the Multiplexer 2 clocked outputs*/

wire metal 187,894 w 4 d 69.5
  diff w 4 d 16
  metal w 4 d 78.5 l 42 d 241 r 150
  poly w 2 u 5;

/*  Connect phase one of the Modclk to the Decoder clocked output  */

wire diff 179,2239 w 4 r 143 d 18
  metal w 4 d 477 r 41
  diff w 4 r 28 d 506 l 90
  poly w 4 u 26;

/*  Connect phase two of the Modclk to the Counter and Multiplexer
    clocked outputs                                                */

wire metal 177,2228 w 4 r 2
  diff 179,2228 w 4 r 129
  metal w 4 d 500 r 7
  poly w 2 d 5;  /*  Phase 2 (PH2) to Multiplexer  */
wire metal 508,2228 w 4 r 52 u 89
  poly w 4 u 22 w 2 l 8;  /*  Phase 2 (PH2) to Counter  */

}

/*************************************************************

     This is the section that generates the brain chip array
(16 X 16) as it interfaces with the multiplexer, and the
outside world.

*************************************************************/

electrode

{

/*  Build the brain chip electrode  */

wire metal 21.5,80 w 90 r 90;
rect 22.5,36 88,88 glass;
wire metal 66.5,35 w 10 d 6;
wire diff 66.5,35 w 10 d 19 w 8 l 9;
wire metal 61.5,14 w 8 l 57.5 d 14 u 125;
rect 58.5,11 2,6 contact;
rect 62.5,30 8,2 contact;
wire diff 0,25 w 4 r 13
  metal w 4 r 43.5
  poly w 4 r 20
```

```
  metal w 4 r 43.5
  diff w 4 r 5;

}

c_bonding_pads

{

/*  Build the brain chip column output bonding pads  */

rect 0,0 115,115 metal;
rect 1,1 113,113 glass;

}

lines

{

wire diff 4,0 w 8 u 156;
rect 1,1 6,2 contact;
rect 1,153 6,2 contact;

}

/*************************************************************

     This is the section that generates the Counter PLA,
with its clocked input and output "registers".  This PLA has
eight inputs and four outputs.

*************************************************************/

counter

{

/*  Make the Counter Pla with input and output buffers  */

a903 (20,20);

/* Insert the PlaClockIn modules, which make clocked input register  */

iterate 8,1 16,58
  PlaClockIn (35,--38);

/*  Insert the PlaClockOut modules, which make the clocked output
    register  */

iterate 2,1 16,57
  PlaClockOut (176,--33);

/*  Connect PLA Vdd and drivers Vdd, and PLA Gnd and drivers Gnd  */
```

```
wire metal 22,20 w 4 d 22 r 13;
wire metal 163,--2 w 4 r 5 d 21 r 8;
wire metal 163,17 w 4 r 10 u 3 d 15 r 8;
wire metal 208,5 w 4 r 5 u 15;

/*  Connect feed back lines  */

wire diff 109,--38 w 2 d 20 r 94 u 21
  poly w 2 u 4;  /*  Present State 3 (PS3) to Next State 3 (NS3)  */
wire diff 109,--56 w 2 d 2
  metal w 4 d 3;  /*  Extend PS3  */
wire diff 125,--38 w 2 d 14 r 70 u 15
  poly w 2 u 4;  /*  Present State 2 (PS2) to Next State 2 (NS2)  */
wire diff 125,--50 w 2 d 2
  metal w 4 d 3;  /*  Extend PS2  */
wire diff 141,--38 w 2 d 8 r 46 u 9
  poly w 2 u 4;  /*  Present State 1 (PS1) to Next State 1 (NS1)  */
wire diff 141,--44 w 2 d 2
  metal w 4 d 3;  /*  Extend PS1  */
wire diff 157,--38 w 2 d 2 r 22 u 7
  poly w 2 u 2;  /*  Present State 0 (PS0) to Next State 0 (NS0)  */
wire diff 157,--38 w 2 d 2
  metal w 4 d 3;  /*  Extend PS0  */

}

/*********************************************************

    This is the section that makes the Decoder PLA,
with its unclocked input "register" and clocked output
"register".  This PLA has eight inputs and one output.

*********************************************************/

decoder

{

/*  Make Decoder Pla with input and output buffers  */

a901 (20,20);

/*  Insert the PlaIn modules, which make unclocked input register  */

iterate 8,1 16,41
  PlaIn (35,--21);

/* Insert the PlaClockOut module, which makes clocked output register*/

iterate 1,1 16,57
  PlaClockOut (176,--33);

/*  Connect PLA Vdd and drivers Vdd, and PLA Gnd and drivers Gnd  */
```

```
wire metal 22,20 w 4 d 22 r 13;
wire metal 163,--2 w 4 r 5 d 21 r 8;
wire metal 163,17 w 4 r 10 u 3 d 15 r 8;
wire metal 192,5 w 4 r 5 u 15;
wire poly 192,18 w 2 r 8;

}

/*************************************************************

     This is the section that generates the Multiplexer PLA,
with its unclocked input "register" and clocked output
"register".  This PLA has four inputs and sixteen outputs.

*************************************************************/

multiplexer

{

/*  Make Multiplexer Pla with input and output buffers  */

a902 (20,20);

/*  Insert the PlaIn modules, which make unclocked input register  */

iterate 4,1 16,41
  PlaIn (35,--21);

/* Insert the PlaClockOut modules, which make clocked output register*/

iterate 8,1 16,57
  PlaClockOut (112,--33);

/*  Connect PLA Vdd and drivers Vdd, and PLA Gnd and drivers Gnd  */

wire metal 22,20 w 4 d 22 r 13;
wire metal 99,--2 w 4 r 5 d 21 r 8;
wire metal 99,17 w 4 r 10 u 3 d 15 r 8;
wire metal 240,5 w 4 r 5 u 15;
wire poly 240,18 w 2 r 8;

}
```

Appendix F

Test and Evaluation of the AFIT Multielectrode Brain Chip Array

This appendix contains a report written by Michael L. McConkey for Dr. Roger Colvin, as a Special Study course at the Air Force Institute of Technology. The figures in the report have been renumbered to match the figure numbering in this thesis. The cifplots of the chip, mentioned in the Introduction, are not included, since the same information can be obtained from Figures 1 and 2, in Chapter I.

Introduction

This report includes the testing of the AFIT multielectrode brain chip array designed by Robert Ballantine, GE-83D. Two generation versions of this chip were designed. Both include the necessary control functions to provide intern al clocking and multiplexing of the electrodes. Both contain a 16x16 array of electrodes. The only difference between the two versions is that one design multiplexes the output so only one electrode is selected at any time, while the other design provides an output of 16 parallel electrodes, plus it contains more output pads that increases the testability of the chip.

Because of this enhanced testability, most of the tests in this report were conducted on this non-multiplexed version. These tests were conducted on subsystems of the design that are common to both versions such as the counter, decoder, and system clock. However, at the end of this report there is a section that covers the functional characteristics of the multiplexed version. Also included at the end of this report are cifplots of each version showing pad identification, sketches of the test equipment layout, and an equipment list.

In order to better understand the explanations for each test, the different pad names are shown in Table IX. These names are used throughout this report.

The tri-state pads, the two phase signals, and the CON signal are not available on the multiplexed version.

Throughout this report, enabling a row will mean supplying a logic 1 signal to the transistor gates on a particular row, and a column output will mean the output from the drain of a particular transistor.

Table IX. Non-multiplexed Chip Pad Names

ϕ1	provides monitoring of 01 clock signal
ϕ2	provides monitoring of 02 clock signal
NCLK	clock input
SYI	sync in (active low)
CS0-CS2	count select
TS0-TS3	tri-state input/output pads
CON	tri-state control signal hi (+5V) - output, count monitor low (gnd) - input, row enable
SYO	sync out (active high)

Procedure

There was no specific procedure that was used for every test. The specific test to be performed dictated the necessary procedure to be used. A general procedure was used throughout, and it simply follows from good engineering practice:

1. All power to the chips should be off while making changes in wire connections.
2. Double check all interconnections to avoid burning out a chip.
3. Calibrate all test equipment before its use.
4. Avoid ground loops in the test structure.

All tests that required a signal injected into the array transistor were done using 1 KHz or 10 KHz sine waves with a chip clock frequency of 1 KHz. This was done to simplify observation of the signals on the oscilloscope because a signal was applied to only 4 out of 64

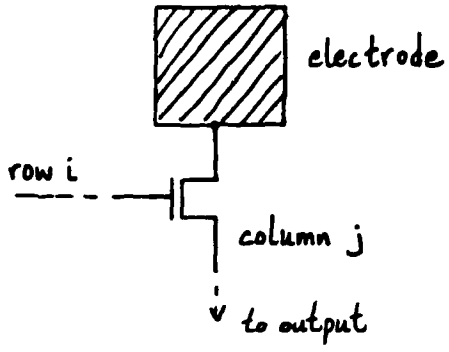


Figure 24. Typical Array Transistor with Electrode

array transistors. Under actual operating conditions, the clock frequency should be at least 800 Hz (16 outputs times 50 Hz sampling of each output). This permits each row to be sampled at least 50 times per second and will prevent any aliasing. For more information on this, see page 33 of Russell W. Hensley's and David C. Denton's thesis, AFIT/GE/EE/82D-29, entitled "The First Cortical Implant of a Semiconductor Multielectrode Array: Electrode Development and Data Collec tion".

Counter Operation

The output of the counter is decoded to provide enabling of a particular row of transistor gates. Figure 24 shows a typical transistor/electrode. All transistors in the array are NMOS enhancement mode devices.

The counter is capable of eight different modes of operation depending upon the status of the count select lines, CS0-CS1, where CS0 is the MSB. Figure 25 shows the different modes of operation and the timing that was observed at the TS0-TS3 outputs with CON at a logic 1.

MODE	CS0	CS1	CS2	COUNT
0	0	0	0	0-15
1	0	0	1	12-15
2	0	1	0	4-7
3	0	1	1	8-15
4	1	0	0	0-3
5	1	0	1	0-7
6	1	1	0	8-11
7	1	1	1	NO COUNT

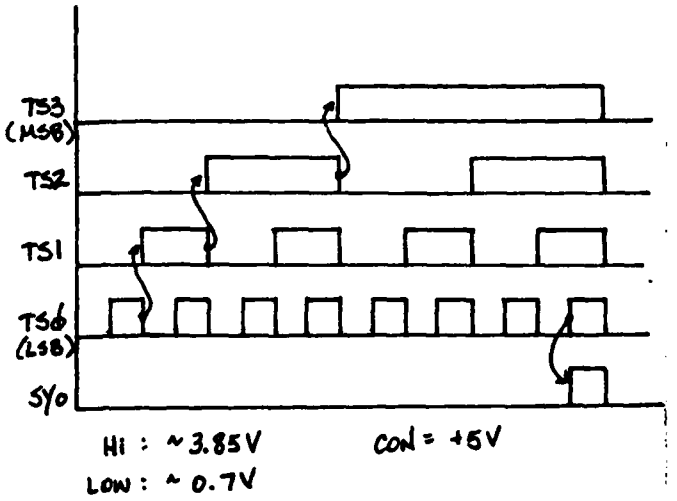


Figure 25. Counter Operation

All eight modes of operation were observed, and all eight modes functioned properly.

The timing diagram shown in Figure 25 is for mode 0.

Multiplexer/Decoder Operation

The multiplexer decodes the count given to it by the counter which selects the proper row to be enabled. The non-multiplexed version provides test points to monitor the signal on each row. Table X shows the observed voltages on each row with the counter set to mode 7, no count. Notice the unusal high voltage on row 1. It is not possible to tell whether this is caused by the counter, decoder, or multiplexer PLAs when the counter is in this mode.

The voltage observed is below the turn-on threshold voltage of the array transistors (except for row 1). This was a problem in the

Table X. Row (Gate) Voltages for Deselected Row

row 1 - 5.76V	row 9 - .465V
row 2 - .417V	row 10 - .437V
row 3 - .469V	row 11 - .467V
row 4 - .425V	row 12 - .429V
row 5 - .476V	row 13 - .467V
row 6 - .424V	row 14 - .434V
row 7 - .480V	row 15 - .466V
row 8 - .425V	row 16 - .431V

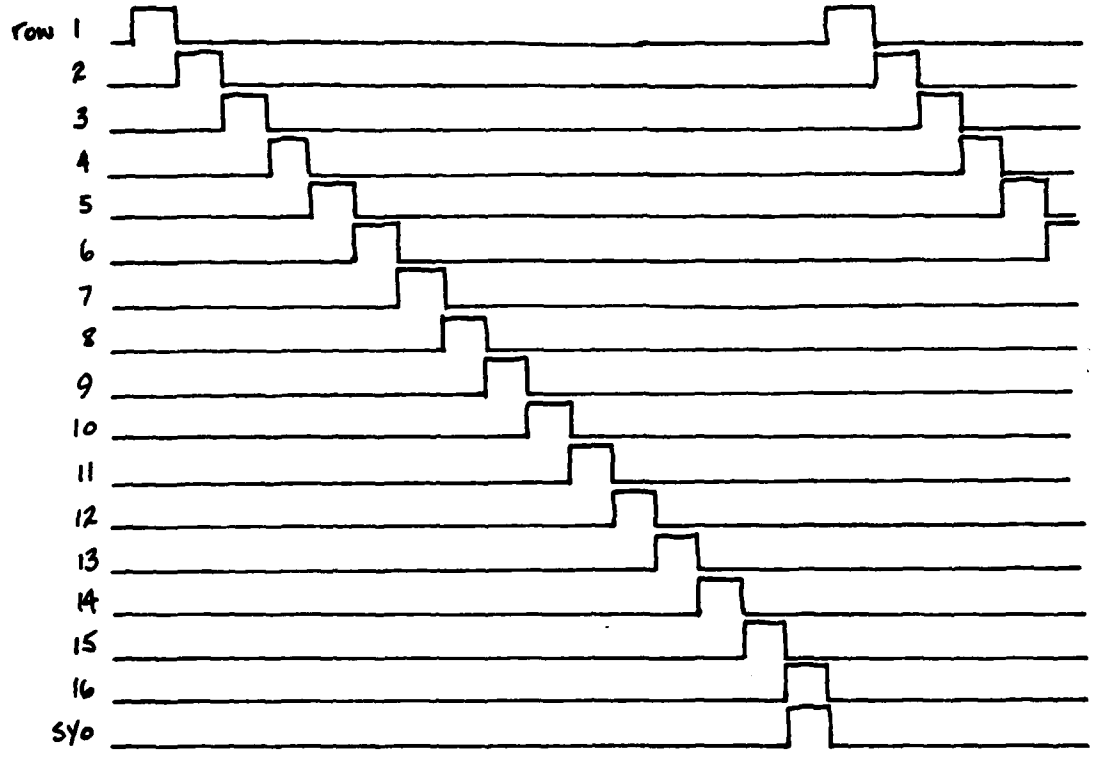


Figure 26. Row Pulses for Array Transistors

original, 1st generation, design.

Figure 26 shows the observed row pulses with the counter set to

mode 0. Notice that row 1 operates correctly. Apparently, the voltage observed for row 1 in Table X occurs only when the counter is in mode 7. This irregularity in the row 1 enabling should be no problem since mode 7 of the counter will probably not be used. Each count mode was observed and each row was enabled correctly for all modes.

Table XI. On and Off Resistances for a Typical Transistor

R	Channel Resistance
10 Kohms	on - 4.7 Kohms off - 360 Kohms
100 Kohms	on - 3.71 Kohms. off - 10.9 Mohms
1 Mohms	on - 3.37 Kohms off - 9.8 Mohms

Array Transistor Characteristics

The DC resistance for a typical transistor in the array was calculated for three different values of load resistance. The "on" resistance and the "off" resistance of the channel was found, and the results are shown in Table XI. The voltage transfer characteristic for a typical transistor is shown in Figure 27. Shown is a curve for each load resistance, R, and the schematic that was used to determine the transfer curves and the "on" and "off" channel resistances. Note: these curves are an average from data collected from ten such transistors. Because the output from each transistor (the drain) is going to drive an operational amplifier, the data collected for the 100

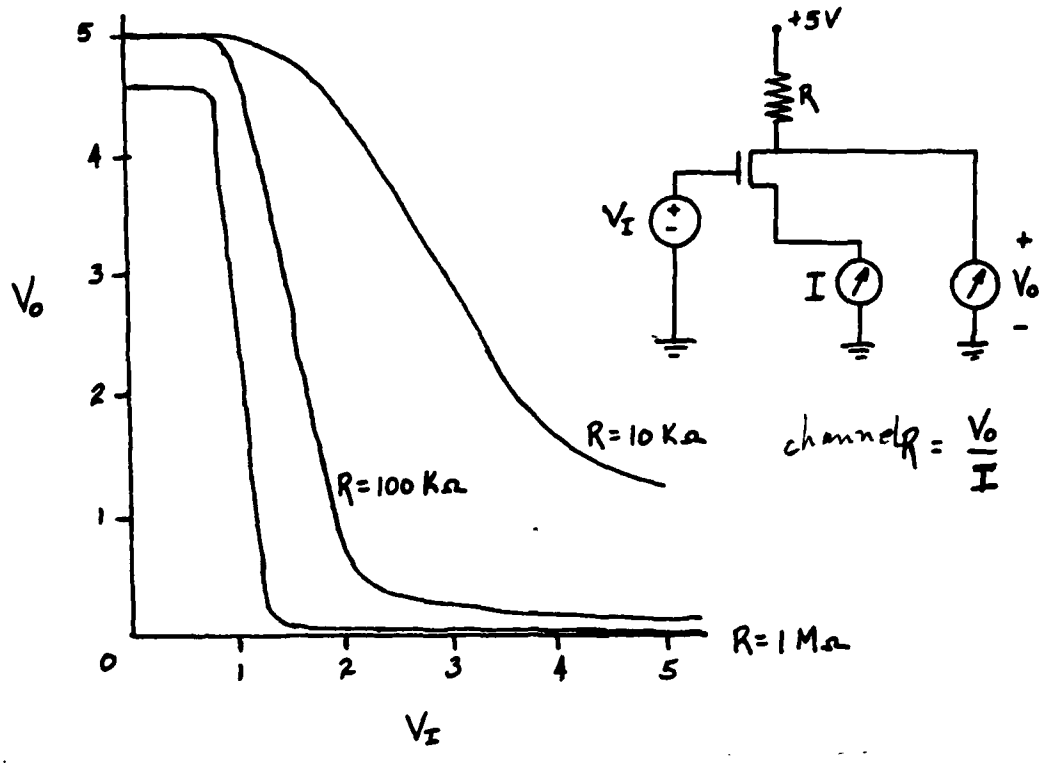


Figure 27. Voltage Transfer Curves

Kohms and the 1 Mohms values of R represent the best approximation for actual transistor operation under normal operating conditions.

Array Transistor Switch Operation

The switch action of a particular array transistor is shown in Figure 28. The counter was set to mode 4 (0 - 3). A 1 KHz sine wave was applied to the source of one transistor and a 10 KHz sine wave was applied to the source of a second transistor in the same column. The figure shows the observed output.

As can be seen from the figure, the transistor switches properly

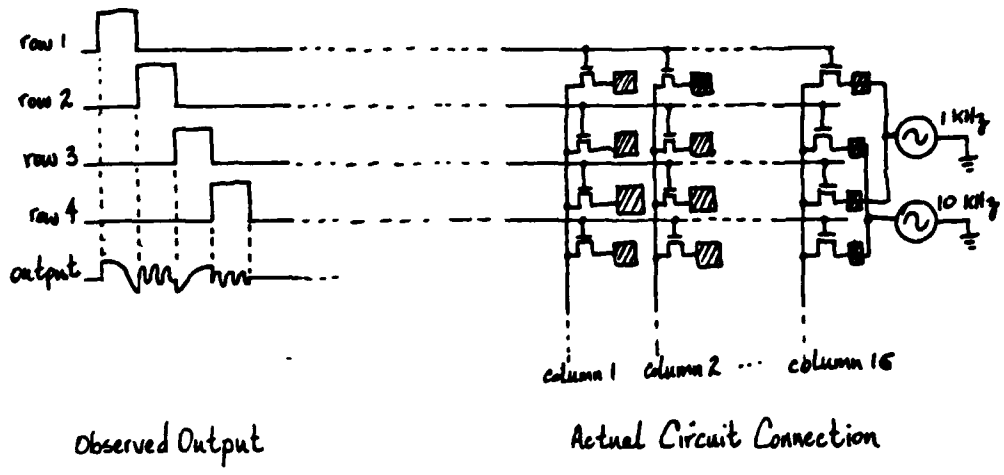


Figure 28. Array Transistor Switch Action

allowing the signal that is present at its source to be sent to the output.

Sync In / Sync Out Operation

Each version of the chip includes a "Sync In" and a "Sync Out" signal connection. When Sync In is low, the chip counter is enabled and the row selection pulse is multiplexed down the array. When Sync In is high, the counter is disabled. Sync Out is pulsed from low to high to low when the counter has reached the end of its count sequence. The top two traces of Figure 29 shows the timing relationship of these two signals. These two signals are used to synchronize the timing of the entire system. They can be used to start and reset measurement devices.

To provide more data collection capability, two or more chips may be cascaded together. Figure 30 shows the interconnection for two

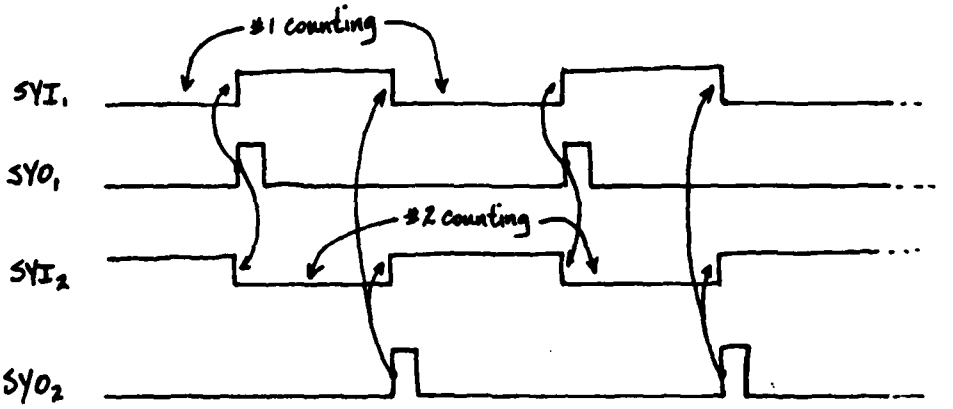


Figure 29. Sync In / Sync Out Timing Diagram

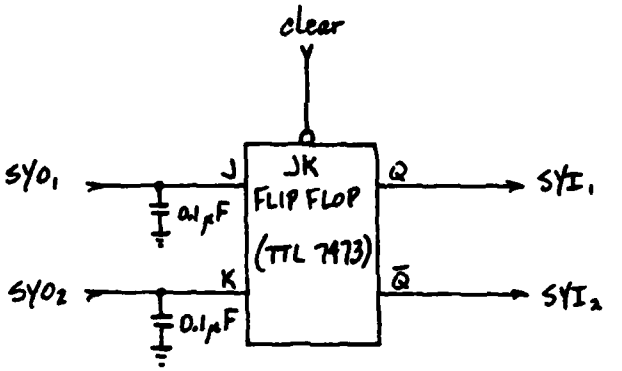


Figure 30. Circuit Required to Cascade Two Chips

chips. Upon power-up of the system, the "clear" line should be pulsed from high to low to high to ensure that counting starts with chip number 1. At any time during operation, the "clear" line can be pulsed to reset the system. The capacitors on the inputs are neccessary to prevent erroneous switching. Correct synchronization operation using the circuit of Figure 29 was verified for all modes of the counter.

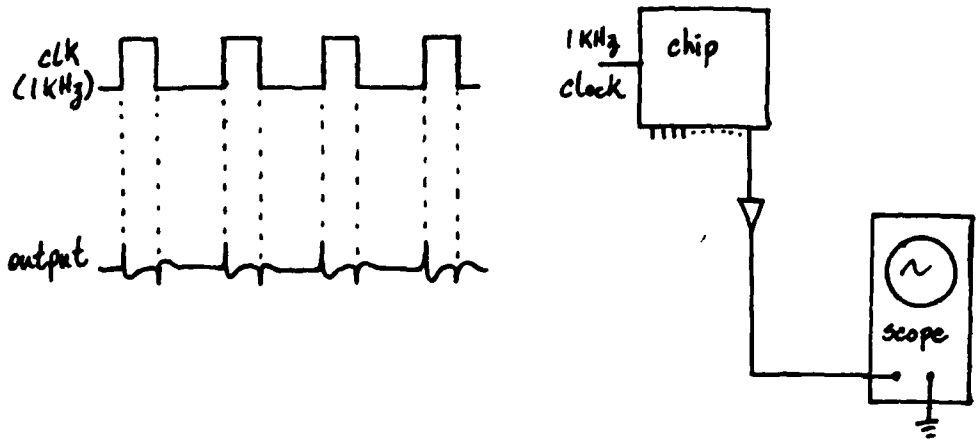


Figure 31. Observed Noise on Output

Noise Measurements

For this section, a uA741 operational amplifier configured as a single-ended, noninverting amplifier with gain of 100 was used to make the measurements. Figure 31 shows the observed output at a drain of the test transistor with no sine wave applied to the source. This noise is caused by the switching of the clock pulse, not the gate pulse. This can be deduced because the observed noise is at the clock rate rather than the gate pulse rate which is a factor of two slower. Because the clock switches at a relatively high frequency as compared to the expected frequency of brain wave activity, a small bypass capacitor applied across the output to ground can be used to eliminate this noise. The capacitor used in this experiment was 0.1 uF which sharply attenuated the noise to an immeasurable value for this test set-up.

By adding 1 KHz and 10 KHz signals to the source of two transistors in the same column, Figure 32, the following was observed. The bypass capacitor permitted the 1 KHz sine wave signal to pass through, but it

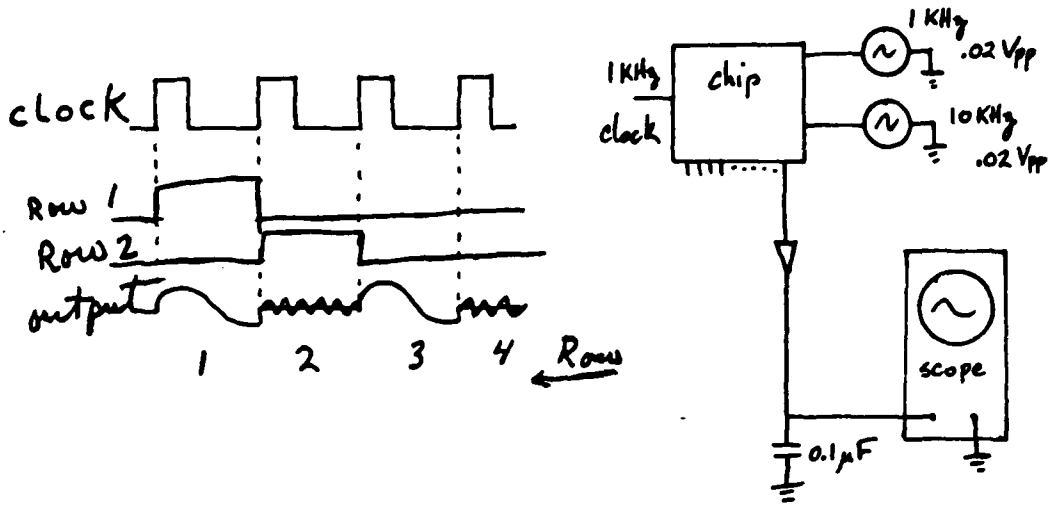
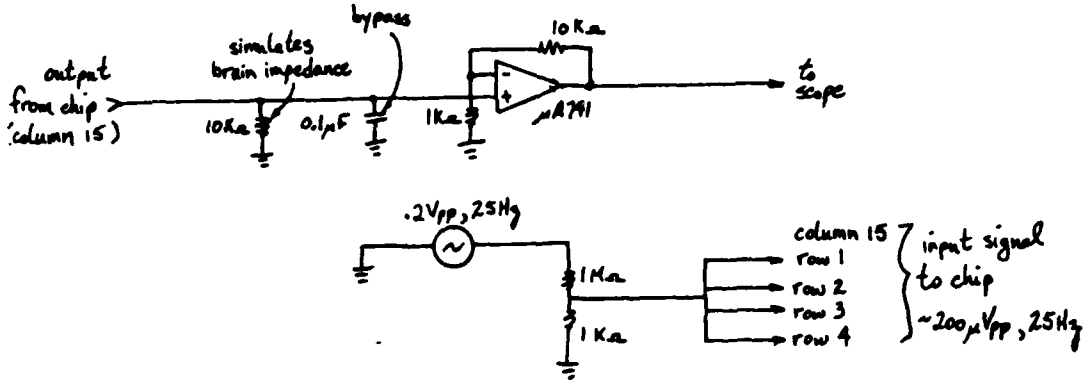


Figure 32. Observed Output with Bypass Capacitor

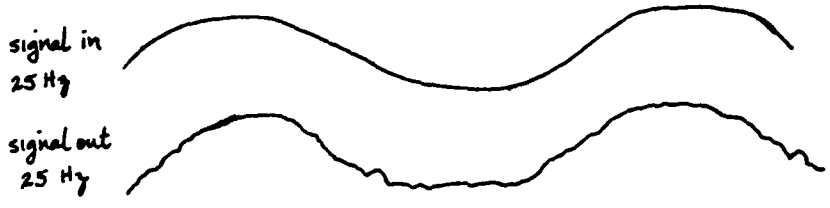
sharply attenuated the 10 KHz sine wave. This should pose no problem as the maximum brain wave frequency is 25 Hz.

Frequency crossover was also measured for both the 1 KHz signal and the 10 KHz signal. One signal was applied to the source of a transistor that was always on, and the other signal was applied to the source of a transistor in the same column that was always off. Both transistors resided in the same column and the bypass capacitor was not used. Both signals showed a crossover ratio of approximately 30:1 (signal in to signal out) which is about 29.5 dB crossover rejection.

Also measured was the ratio of the magnitude of the signal in to the magnitude of the same signal out without the bypass capacitor. For a 1 KHz sine wave input, the output was attenuated 1.15 dB. For a 25 Hz signal input, no noticeable attenuation was observed. All measurements so far were taken at the drain of the test transistors. Measurements at the source of the test transistors showed no noticeable



a) Schematic



b) Observed Output

Figure 33. Brain Simulation Model

feedthrough or switching transients.

Brain Simulation

Because this multielectrode array has to measure signals on the order of a few tens of microvolts, a simulation of the brain was necessary to determine the array's effectiveness at measuring such low signals while at the same time rejecting noise. Figure 33 shows the model and schematic used. Also shown is the observed signal in and signal

out. These measurements were made with the counter in mode 4, counting 0-3, and a 200 +Vpp 1 KHz sine wave applied to four transistors in the same column within the array. The same test was performed with the sine wave applied to only one transistor, and the appropriate segment of the same output was observed when the transistor gate was pulsed.

All switching transients were negligible. The 60 Hz noise observed at the output will not be present under actual operating conditions because shielded cable and batteries will be used.

Interface Circuitry

Denton and Hensley designed an external drive circuit for the first generation brain chip. This circuitry was designed to provide clocking, multiplexing, and syncronization for a 4x4 array. This circuitry can still be used for connecting the new array to data recording devices as shown in Figure 34. For more detail concerning this external

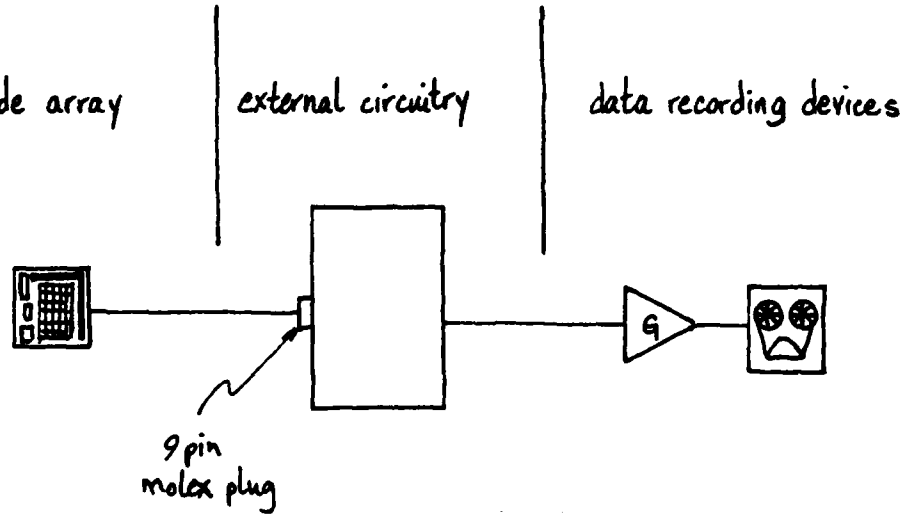


Figure 34. Interface Schematic

drive circuit, see Denton and Hensley's thesis, AFIT/GE/EE/82D-29.

Depending on which 2nd generation chip is used for the data collection will dictate how the connection between the circuitry and the array should be made. If the multiplexed version is used, then the output from the array can be connected to any one of the four inputs in the back of the chassis and the corresponding output from the chassis can be connected to the data recording devices. If the non-multiplexed version is used, then there exists only the capability to measure four out of sixteen outputs. These four outputs will connect directly to the four inputs in the back of the circuit chassis.

The clocking provided by this circuitry cannot be used because the 2nd generation chips provide clocking and multiplexing of their own on the chip. The strobe out and external sync provided by the circuitry must also be ignored because the array has its own clock and generates its own sync out.

The external drive circuitry contains an internal switch that allows single-ended or differential amplification. Figure 35 shows the switching arrangement.

Data Amplification

To record the data it must be amplified. There are two possible methods of amplifying this analog data; either single-ended or differential mode. The amplification used for the brain simulation section of this report was a single-ended amplifier, Figure 36a. Tests were also performed using a differential mode amplifier, Figure 36b. These tests simply include the same ones used in testing the transistor switch action of Figure 28. Figure 37 shows the observed output from this test.

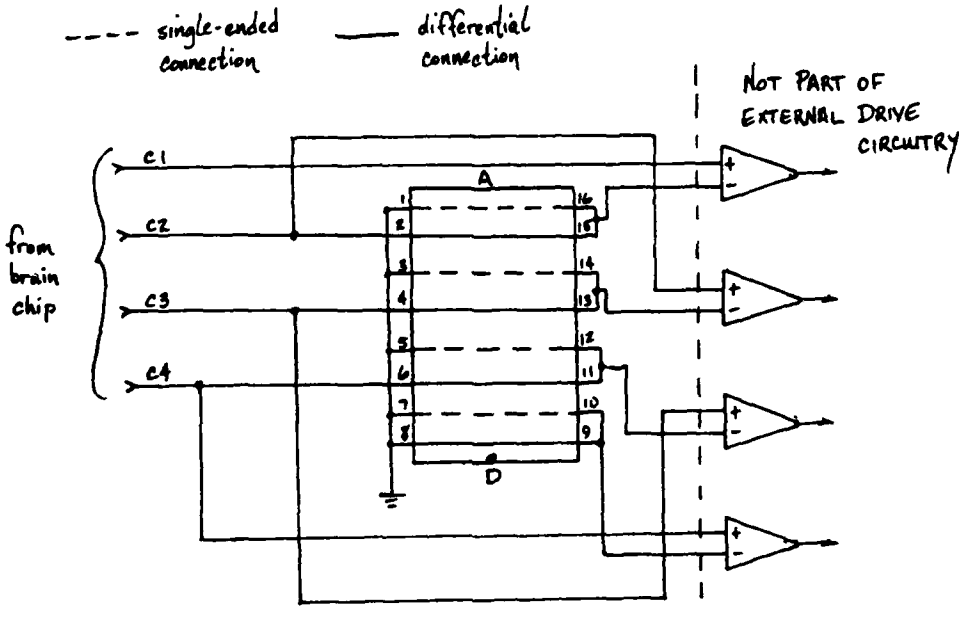
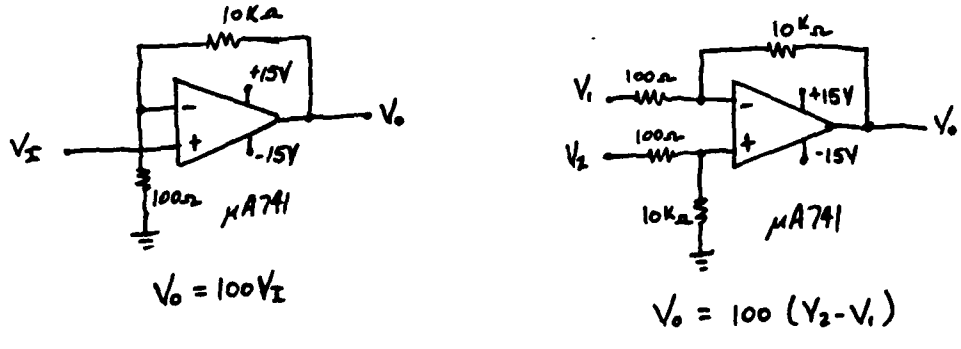


Figure 35. Single-ended and Differential Mode Amplification Connections



a) Single-ended b) Differential

Figure 36. Amplifiers Used in Tests

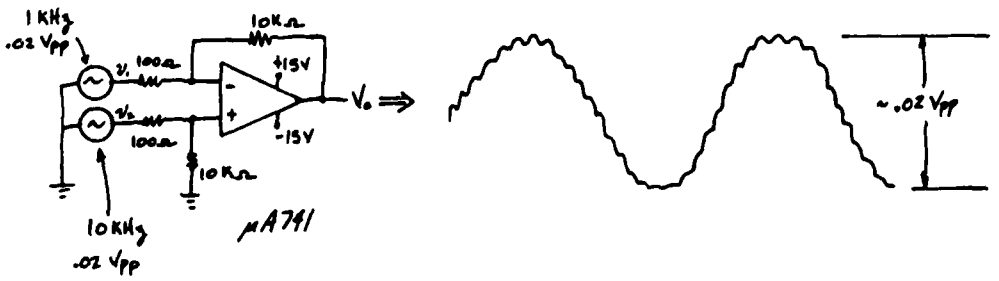


Figure 37. Observed Output Using Differential Amplifier

The actual amplifiers that will be used for data collection are high gain, high noise rejection amplifiers: Princeton Applied Research 113 differential amplifiers.

Multiplexed Version

This version of the chip was tested using the circuit of Figure 32. Testing showed that Sync Out stayed constant at 0V and therefore did not work at all. Also, the output was not timed properly. For all modes of the count select, the output did not change. Instead of reflecting the proper counting sequence, the output showed no signal for 16 clock cycles, then the 10 KHz signal output for 1 clock cycle, no signal for 1 clock cycle, then the 1 KHz signal output for 1 clock cycle, regardless of the count sequence chosen (see Figure 38). These results indicate that the row multiplexor runs twice as fast as it actually should. Improper pad assignment was suspected, but subsequent analysis showed this was not the case. Analysis of the chip itself using a microscope was performed by Dr. Roger Colvin. He concluded

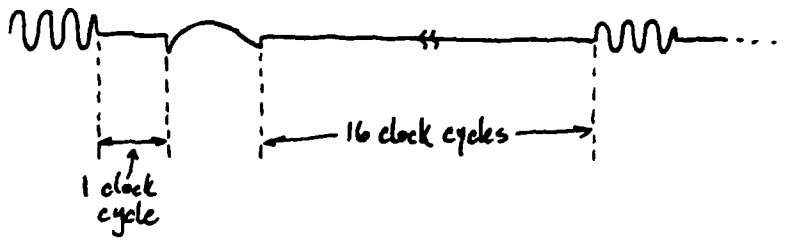
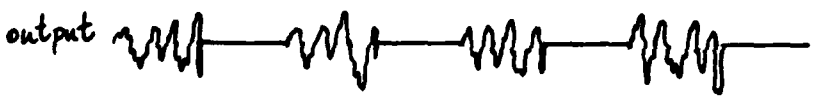


Figure 38. Observed Output, Multiplexed Version from Old Batch

that there was a missing Vdd line for the secondary clocking for the row multiplexor, and that this clocking was not being incremented by the column multiplexor (see the plot in the Appendix).

The same type of chip but from a different batch that had the missing Vdd line was bonded and the same tests performed on it. This new chip behaved entirely different from the old chip. Figure 39 shows the observed output and Sync Out. There were two types of Sync Out observed and both are shown in Figure 39b and 39c. Figure 39b was observed for all count sequences that did not include counting to 15, while Figure 39c was observed for only 4 the count sequences that did include counting to 15.

Two specific problems can be found with this new version: first, there is extra noise on the output due to capacitive pickup; second, Sync Out does toggle when the count sequence includes 15, but it should toggle on the row counter cycles and not on the column counter cycles. Also, Sync Out should remain low and pulse to high at the end of the count sequence instead of toggling half high - half low.



a)Observed Output

b) Sync Out not including count 15

c) Sync Out including count 15

Figure 39. Observed Output, Multiplexed Version from New Batch

Conclusions and Recommendations

The nonmultiplexed version of the chip works very well. The "off" voltage of the rows is sufficiently less than the threshold voltage of the array transistors to prevent unwanted turn-on. This was a problem in an earlier version of this chip. Under actual operating conditions, this chip should work very well as shown in the Brain Simulation section of this report.

The multiplexed version of the chip has problems. The results obtained from testing are not conclusive, but if the problem with Sync Out can be found and corrected, then the total operation of this chip version would probably be correct.

Therefore, the non-multiplexed version should be used for any data collection until the problems with the multiplexed version can be analyzed and corrected.

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Vita

Captain Ricardo R. Turner was born in Bourne, Massachusettes, August 31 1955. He graduated from Clover Park High School in Tacoma, Washington, in 1973. He attended the United States Air Force Academy from 1973 through 1977 where he received a Bachelor of Science degree in both Computer Science and Mathematics (Operations Research). Upon graduation from the Air Force Academy, he was commisioned as an officer into the United States Air Force. His first Air Force assignment was at Mather AFB, California, where he attended Undergraduate Navigator Training. After receiving his Navigator Wings in 1978, he attended Electronic Warfare Officer Training at Mather AFB. As his first operational assignment, Captain Turner flew the B-52D as an Electronic Warfare Officer (EWO), Instructor EWO, and Flight Examiner in the 60th Bombardment Squadron, Andersen AFB, Guam. In 1982, he worked as the Chief of Defensive Systems Training Devices for the 43rd Strategic Wing at Andersen AFB. In May 1983, he was assigned to the Air Force Institute of Technology as a graduate student. Captain Turner's permanent address is:

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A 16 X 16 multielectrode semiconductor array, known as the AFIT brain chip, must be encapsulated prior to implantation into the cerebral cortex of a rhesus monkey. The encapsulant, which must protect the chip from the saline-like solution of the cerebro-spinal fluid, was a polyimide: Dupont PI 2555. The polyimide was spun onto the chip, and the electrode openings etched, using negative photolithography and wet chemical etching. An eight-micron thick layer of polyimide was obtained by repeating this process several times. Although actual implantation was not performed, an implantable package was designed and fabricated which will allow for chronic use with only one surgical operation. A surgical technique for implanting the package is suggested. The fabricated package was not fully functional, however, because an epoxy used to protect bond wires from the stress of the polyimide could not withstand the high temperature cure. The functioning part of the chip was tested in vitro and worked continuously for three weeks. There was no damage to the polyimide encapsulant, but some of the aluminum electrodes showed signs of deterioration.

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